



# The Mu3e Data Acquisition System

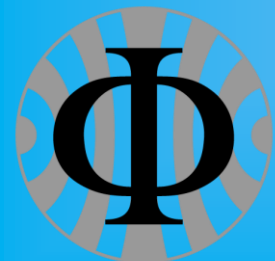
– Handling Terabits per second without hardware trigger –

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on behalf of the Mu3e Collaboration

Physikalisches Institut – Heidelberg University

*IFDEPS – Annecy – 13.03.2018*



INTERNATIONAL  
MAX PLANCK  
RESEARCH SCHOOL

PT  
FS

FOR PRECISION TESTS  
OF FUNDAMENTAL  
SYMMETRIES

# Trigger-less DAQ in HEP

- Trigger-less:
  - Without hardware trigger
  - Software-only event selection
- Data Acquisition challenges:
  - High resolution  
Detectors with millions of channels
  - High luminosities/rates  
Fast detectors, fast signal processing
  - High data throughput
- Why trigger-less data acquisition?
  - Improve "trigger" efficiency (e.g. LHCb Run III upgrade)
  - High statistics required  
for precision experiments (e.g. PANDA, Mu3e)





# The Mu3e Experiment

Search for the charged lepton flavor violating decay  $\mu^+ \rightarrow e^+ e^- e^+$

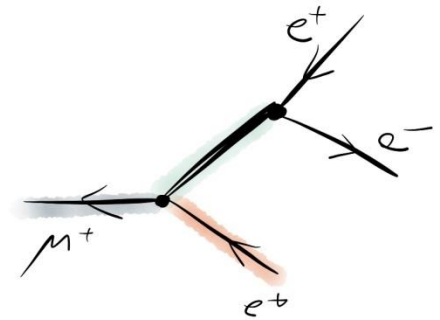
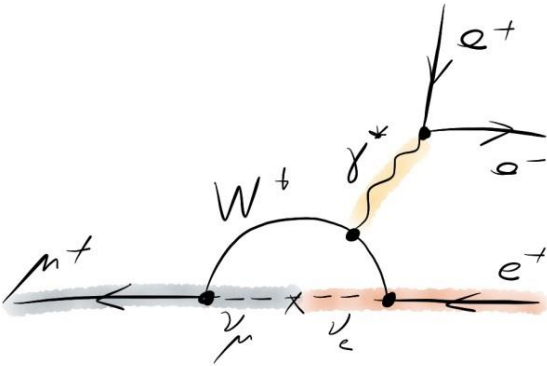
## Standard Model

Highly suppressed branching ratio

$$\mathbf{BR_{SM} < 10^{-54}}$$

## Probe physics beyond SM

Any observation is a clear sign  
for **new physics!**



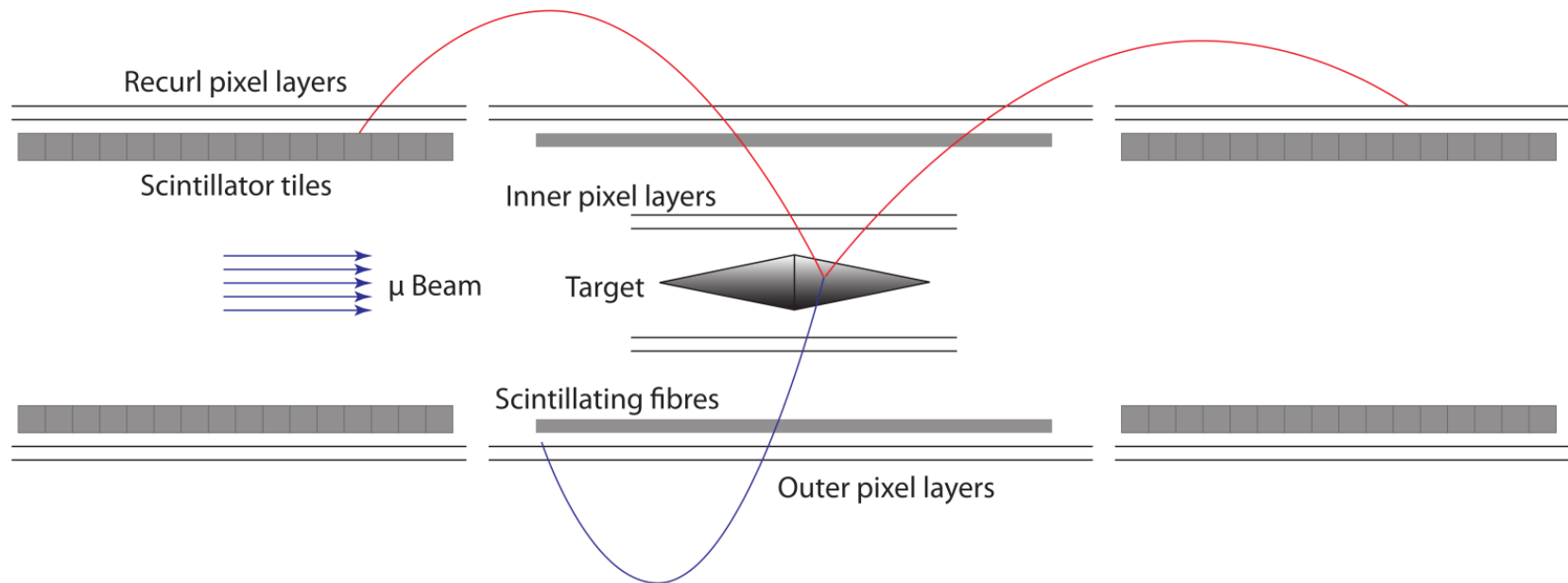
Current limit on  $\mu^+ \rightarrow e^+ e^- e^+$   $\mathbf{BR_{meas} < 10^{-12}}$  (SINDRUM 1988)

## Goal of Mu3e

Enhance sensitivity to branching ratios  $\mathcal{O}(10^{-16})$



# The Mu3e Detector

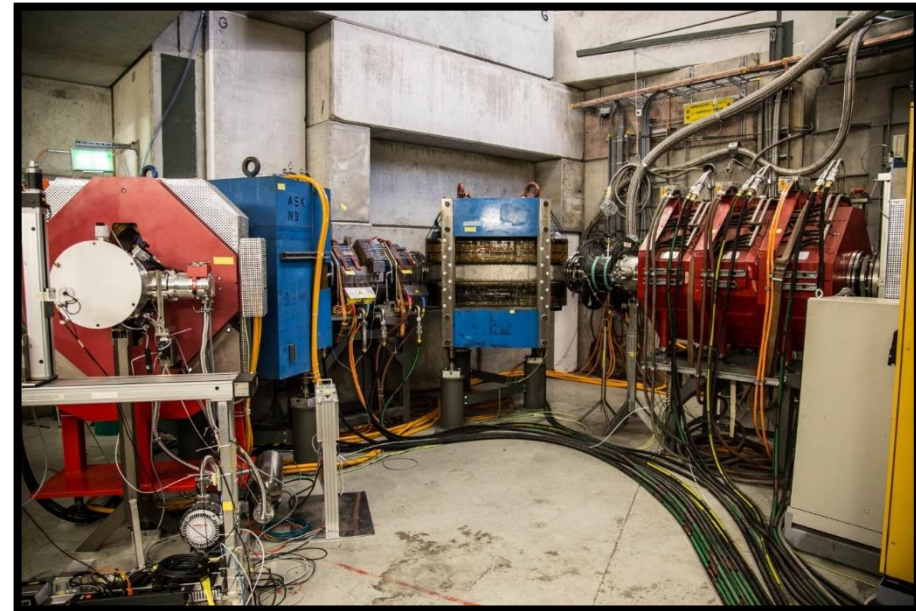


- Stopped muons decay in a solenoidal magnetic field of  $B = 1T$
- Low momentum electrons:  $p_e \leq 53 \text{ MeV}/c$
- **Thin silicon pixel tracking detector:**  
precise momentum ( $\sigma_p < 1.0 \text{ MeV}/c$ ) and vertex ( $\mathcal{O}(100 \text{ } \mu\text{m})$ ) measurement
- **Scintillating fibres and tiles:** precise time information ( $\sigma_t < 500 \text{ ps}$ )



# An Experiment at the Intensity Frontier

- For the final sensitivity goal of  $\mathcal{O}(10^{-16})$  we need to observe  $\mathcal{O}(10^{16})$  events
- High rate of muons, available at Paul-Scherrer-Institut (CH)
- Phase I:  $\mathcal{O}(10^8 \text{ s}^{-1})$ :
  - Existing Compact Muon Beamline
  - Single event sensitivity goal:  
 $2 \times 10^{-15}$
- Phase II:  $\mathcal{O}(10^9 \text{ s}^{-1})$ :
  - Future High Intensity Muon Beamline
  - Under investigation
  - Sensitivity goal:  $\mathcal{O}(10^{-16})$







# An Experiment at the Intensity Frontier

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## ○ Phase I: $\mathcal{O}(10^8)$

Measure and reconstruct all events

- Existing  $\mathcal{O}(10^8)$   $\mu$  beamline  $\blacktriangleright$  Trigger-less data acquisition
- Single event  $\blacktriangleright$  Continuous readout of the full detector
- $2 \times 10^8$   $\blacktriangleright$  Online event reconstruction and filtering

## ○ Phase II: $\mathcal{O}(10^9 \text{ s}^{-1})$ :

- Future High Intensity Muon Beamline
- Under investigation
- Sensitivity goal:  $\mathcal{O}(10^{-16})$





# Readout Bandwidth Requirements

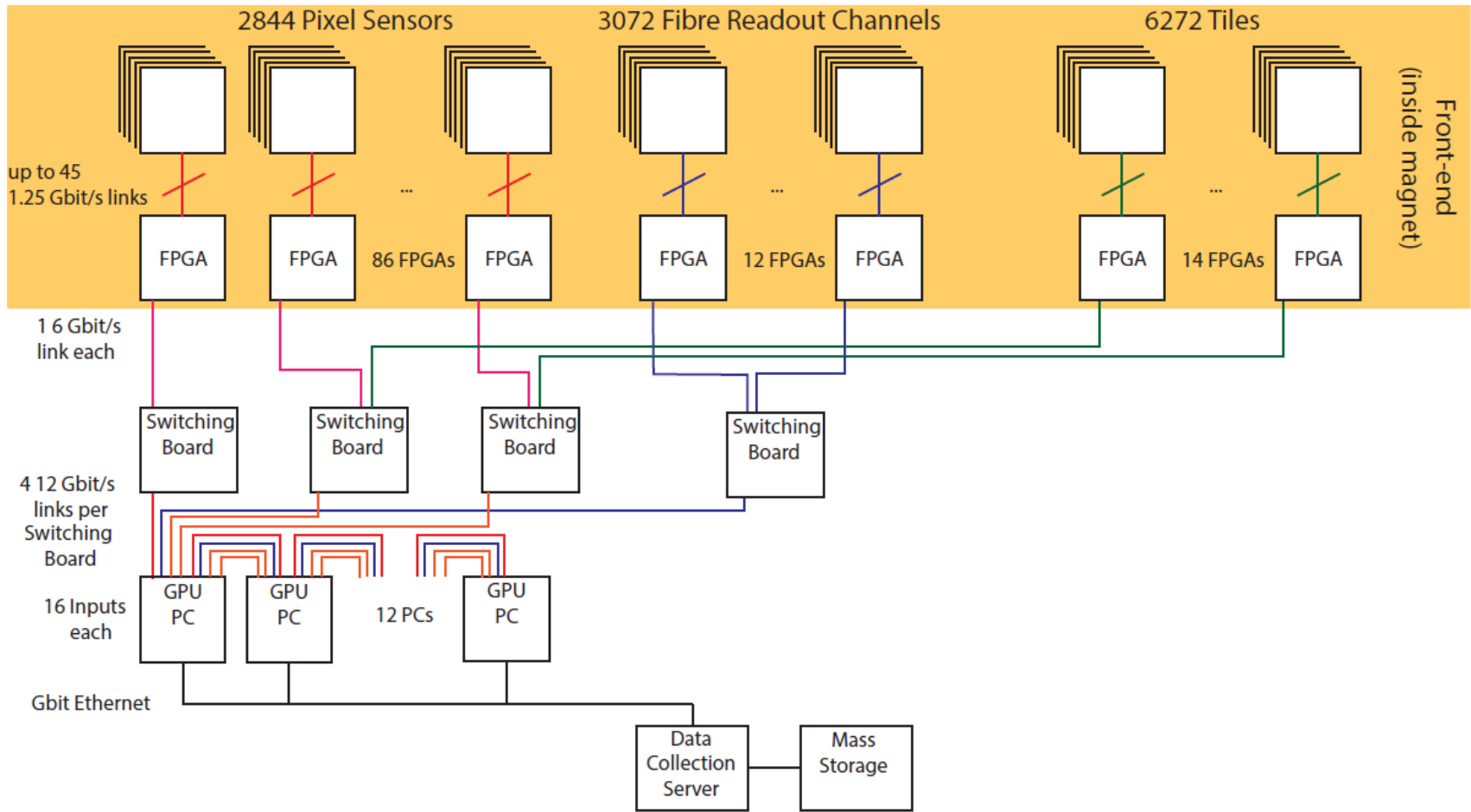
- Hit rates derived from full detector simulation
- Pixel detector only: 2844 sensors = 178 MPixel
- Hit rates increase by a **factor of 20** for Phase II

Muon stopping rate (Phase I)	100 MHz
Maximum hit rate of the busiest pixel sensor	1.5 MHz/cm <sup>2</sup>
Average total pixel hit rate	1.06 GHz
Data rate due to pixel hits (32 bits per hit)	34 Gb/s
Data rate due to pixel noise	5.7 Gb/s · $R_{noise,pix}/\text{Hz}$
Total readout bandwidth	3.8 Tb/s

$R_{noise,pix}$ : Noise rate per pixel  $\ll$  10 Hz



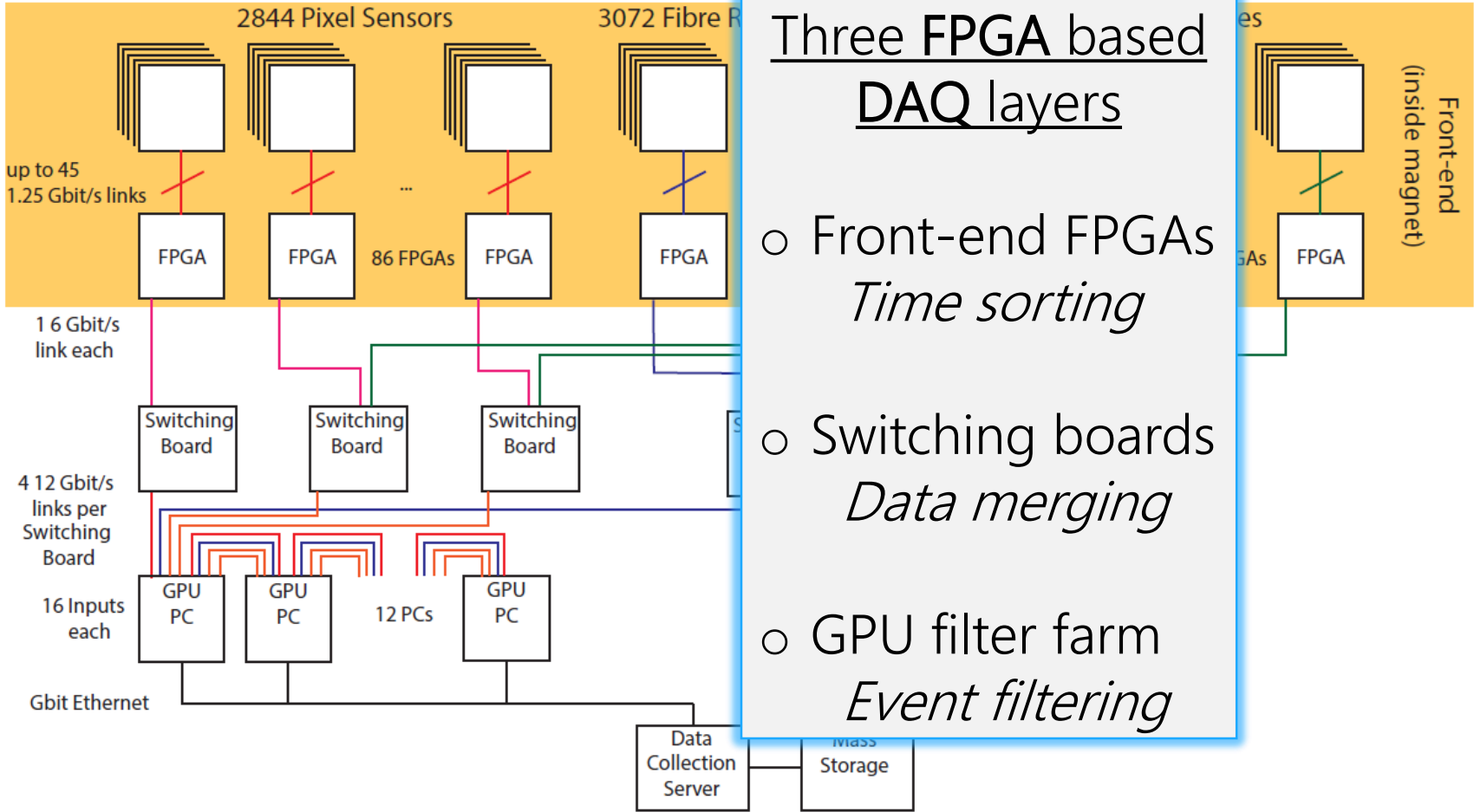
# The Mu3e Readout Concept







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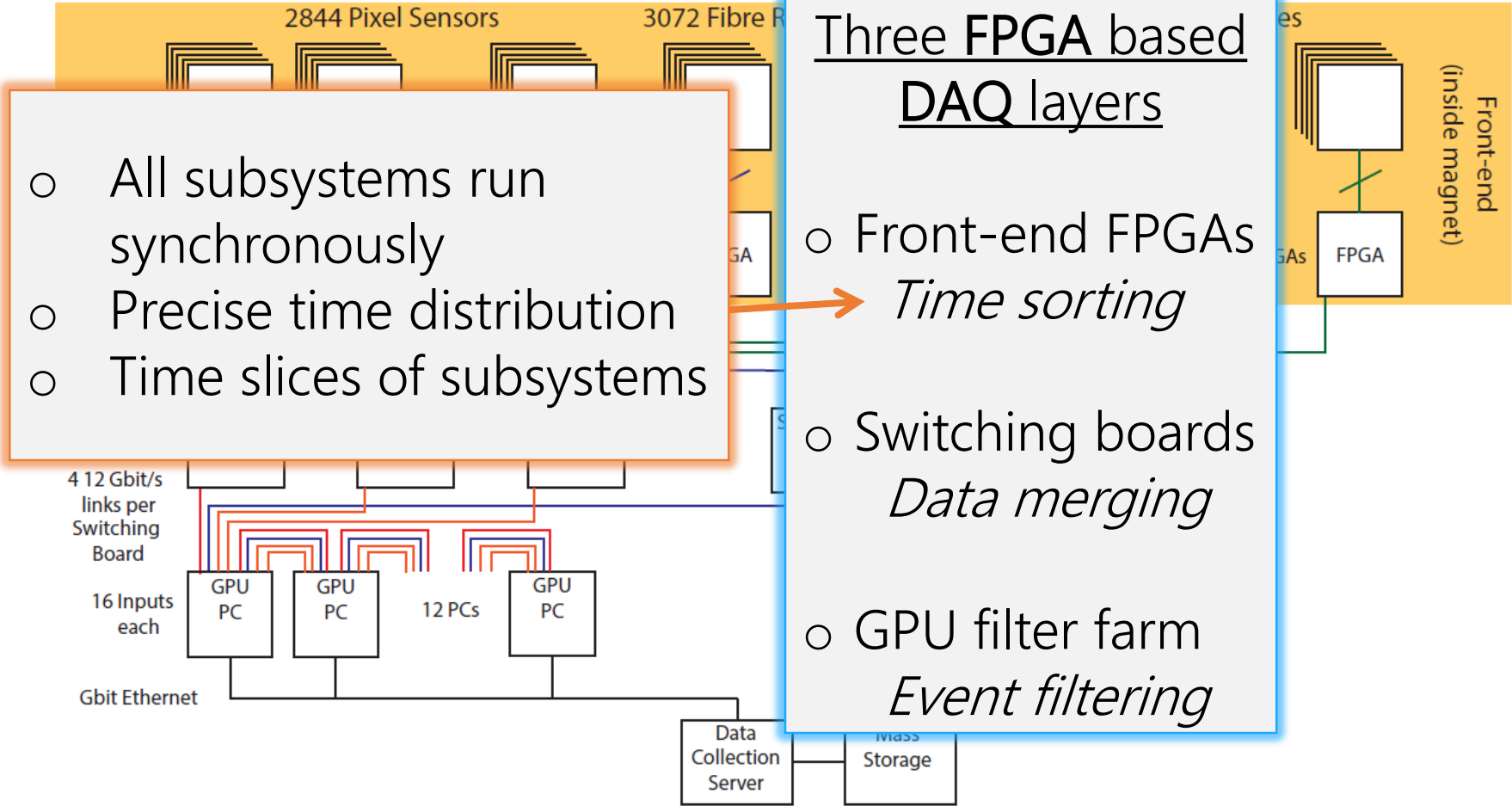


## Three FPGA based DAQ layers

- Front-end FPGAs  
*Time sorting*
- Switching boards  
*Data merging*
- GPU filter farm  
*Event filtering*

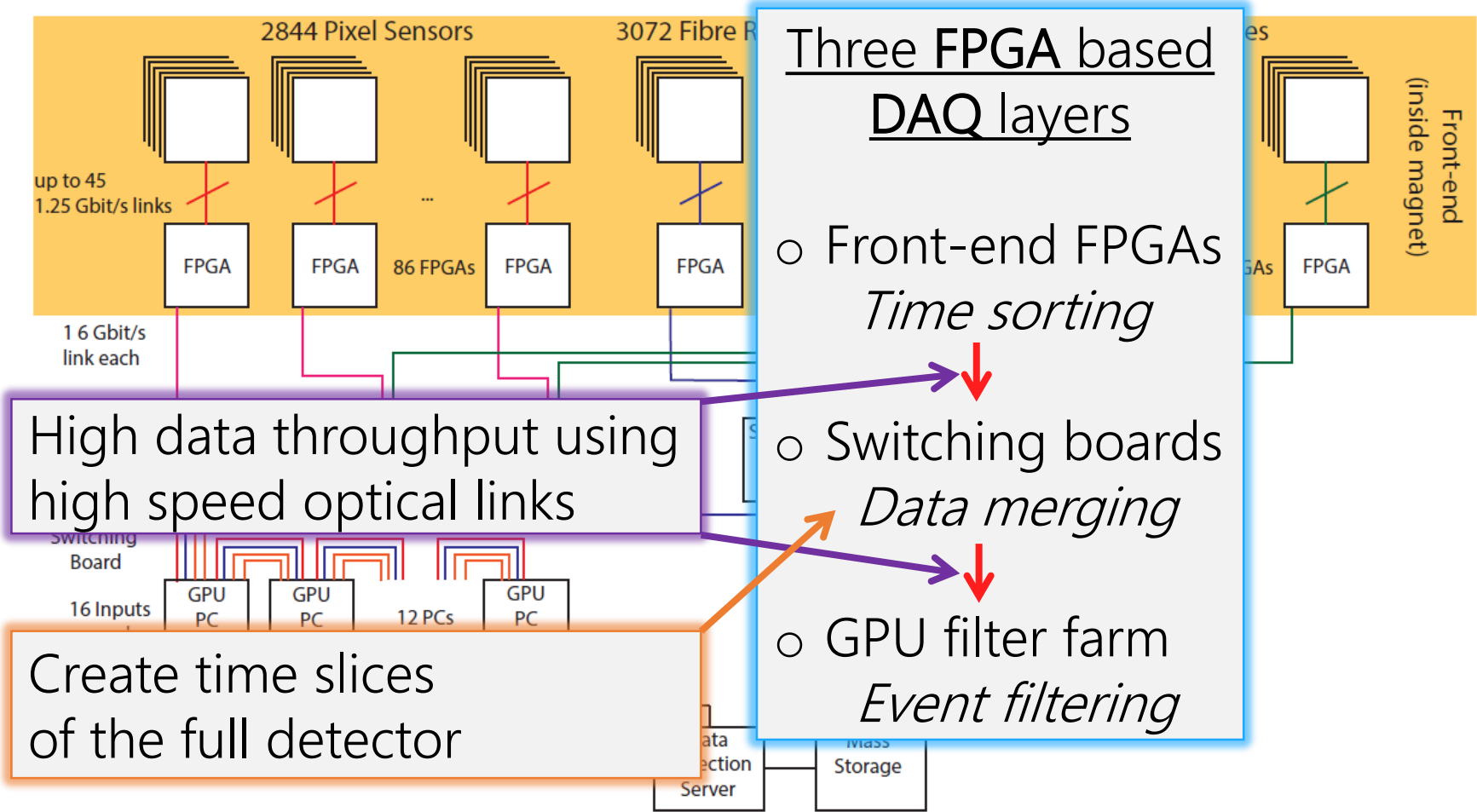


# The Mu3e Readout Concept



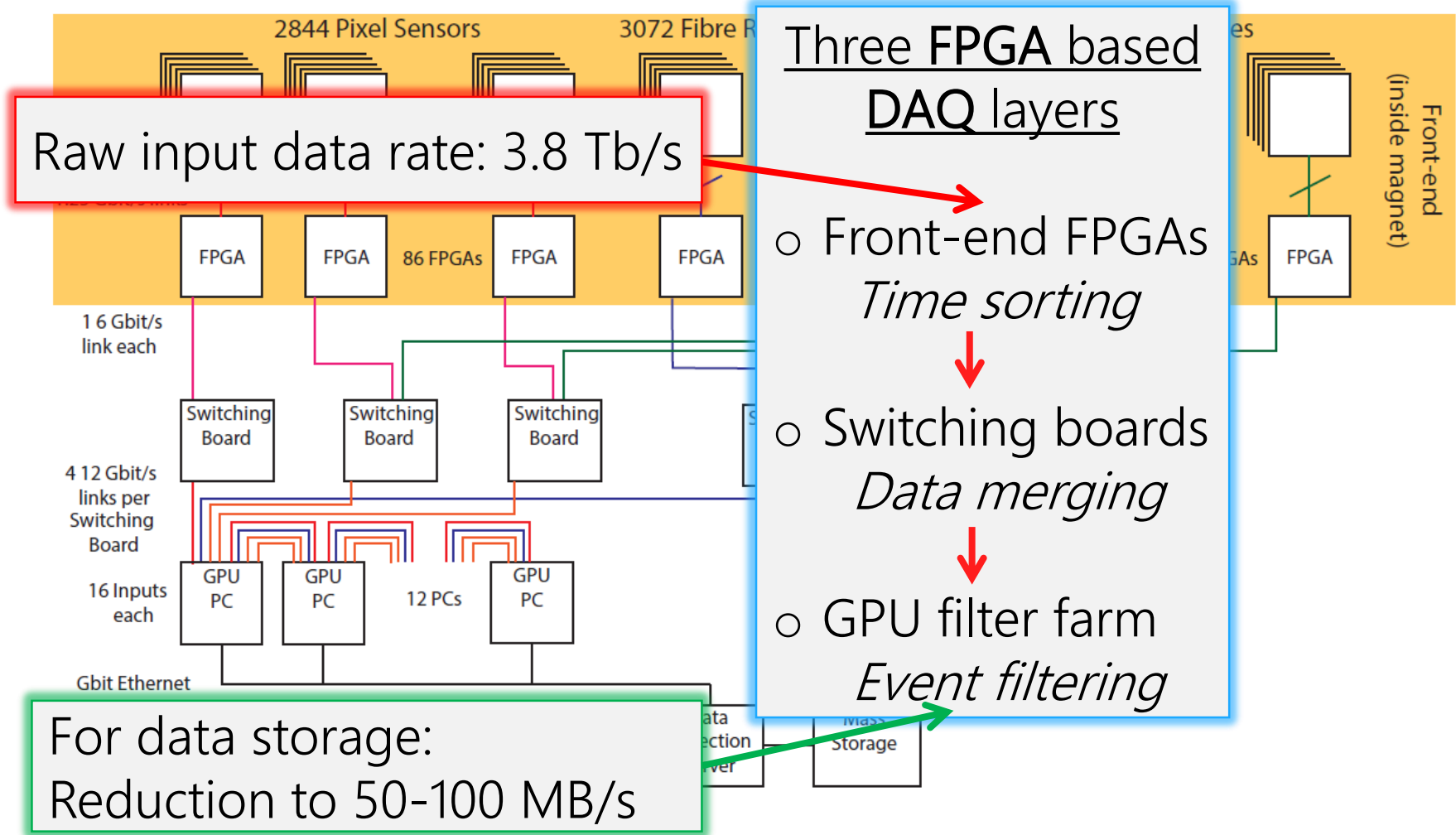


# The Mu3e Readout Concept



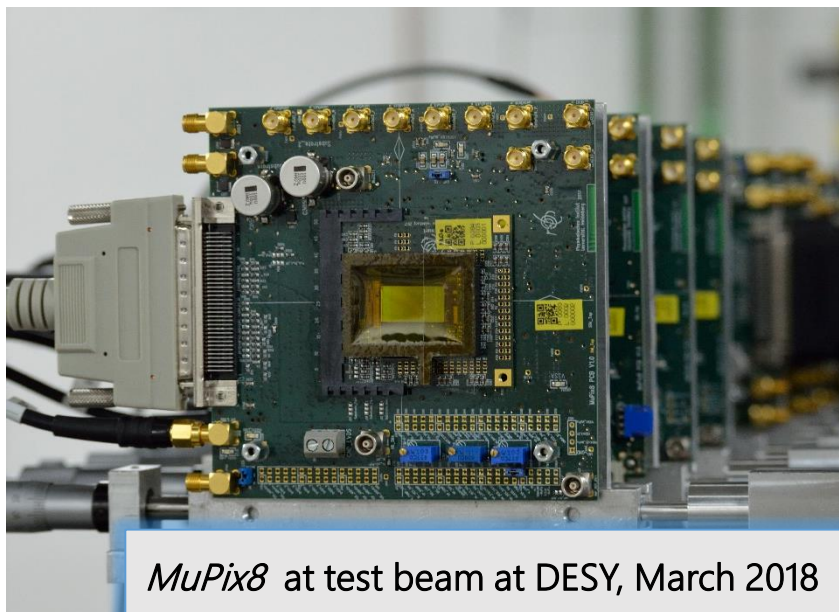


# The Mu3e Readout Concept



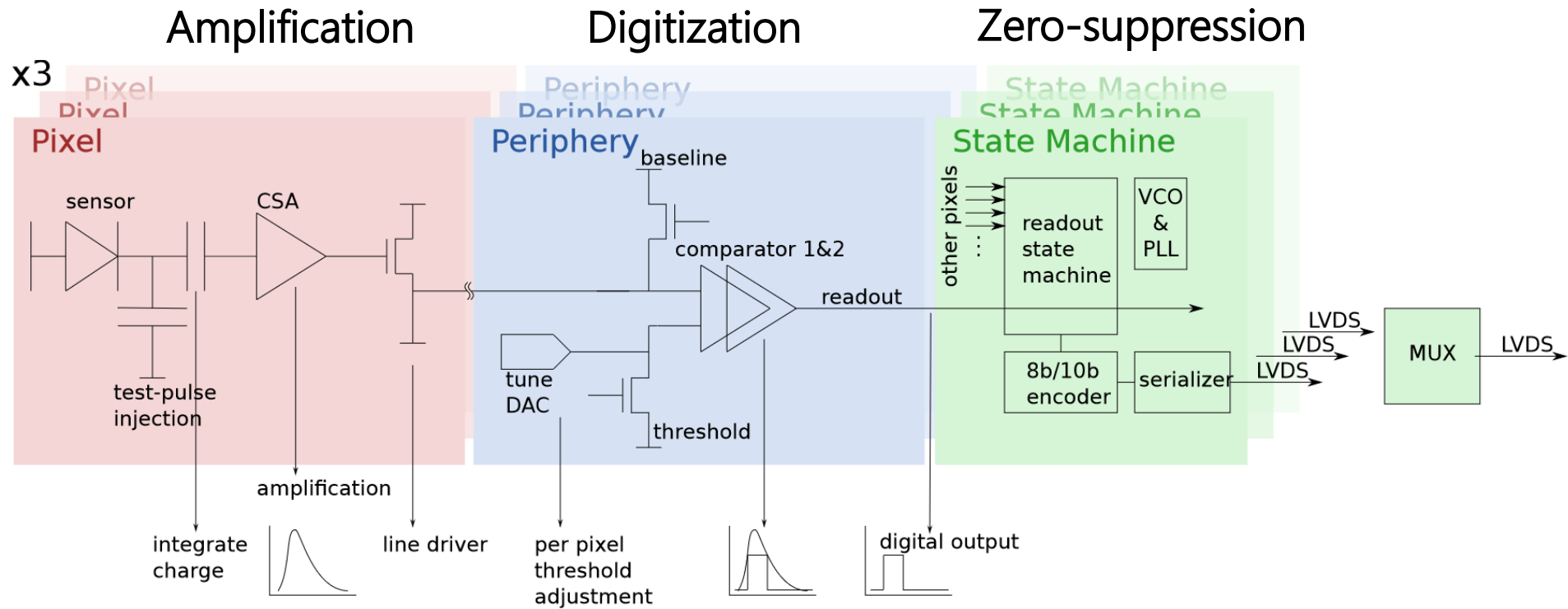
# Mu3e Pixel Sensors – *MuPix*

- High Voltage Monolithic Active Pixel Sensors
- 180 nm HV-CMOS process (AMS AH18)
- Current Prototype: *MuPix8*





# MuPix8 Readout Architecture







# MuPix8 Readout Architecture

Amplification

Digitization

Zero-suppression

x3

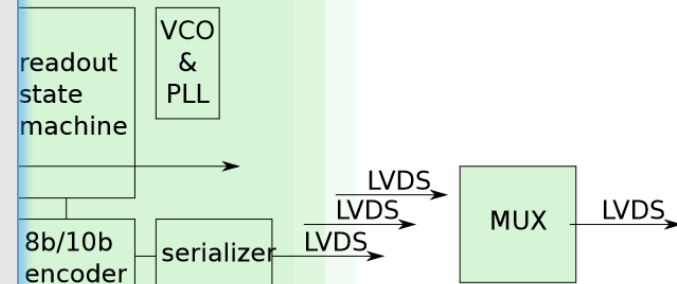
Pixel  
Dival

Periphery  
Periphery

State Machine  
State Machine  
State Machine

- Hits are tagged with an on-chip **timestamp**
- **Position priority based** readout:  
Hit chronology not strictly conserved
- **Trigger-less, continuous** readout
- **Serial data outputs @ 1.25 Gb/s**

adjustment





# MuPix8 Readout Architecture

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Zero-suppression

x3

Pixel  
Dival

Periphery  
Periphery

State Machine  
State Machine  
State Machine

readout  
state  
machine

VCO  
&  
PLL

LVDS

LVDS

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Hit chronology not strictly conserved
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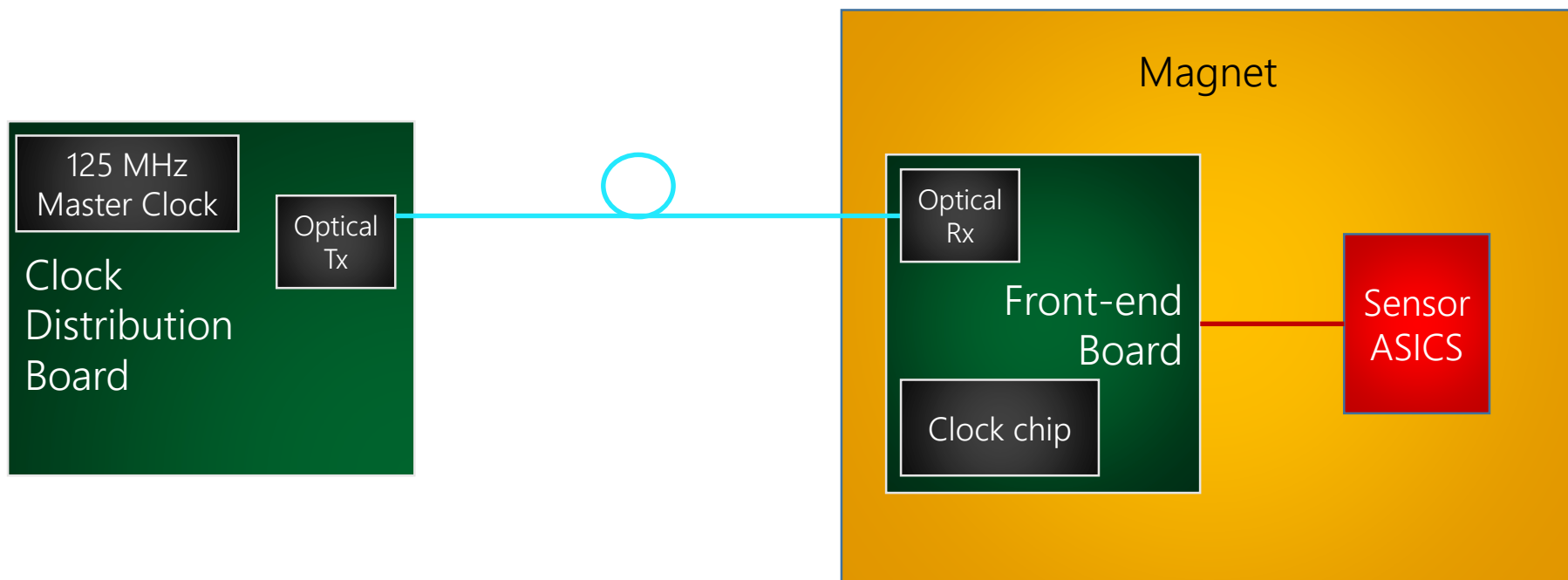
**Precise time  
distribution system!**

adjustment



# Clock and Reset Distribution

- Synchronous timestamps:  
Global synchronous clock and reset signal required
- Custom designed optical clock distribution system

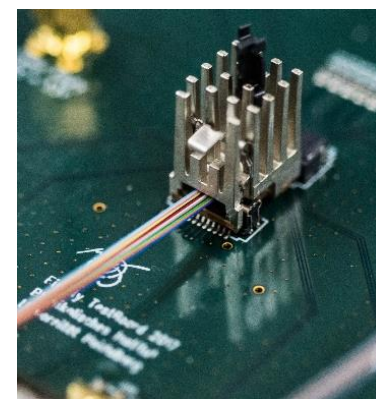






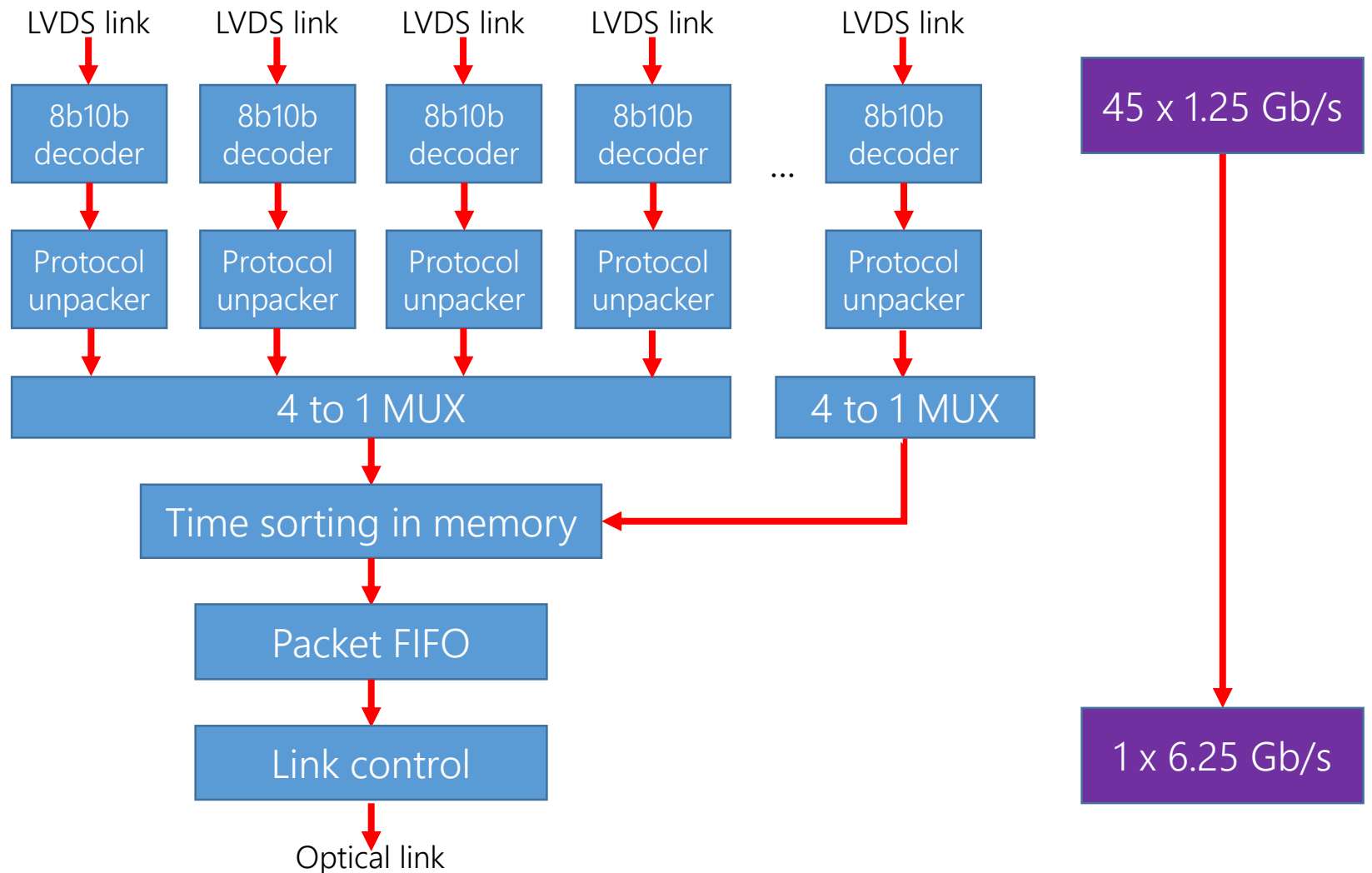
# Mu3e Front-end Board

- Arria V FPGA
- Interface for up to 45 sensors  
LVDS links running at 1.25 Gb/s
- 2 Samtec Firefly duplex x4 transceivers
  - FPGA Multi-Gigabit transmitters at 6.25 Gb/s
  - Receivers: Reset, clock signal, sensor configuration
- Sensor ASIC clock distribution
- First stage of data reduction





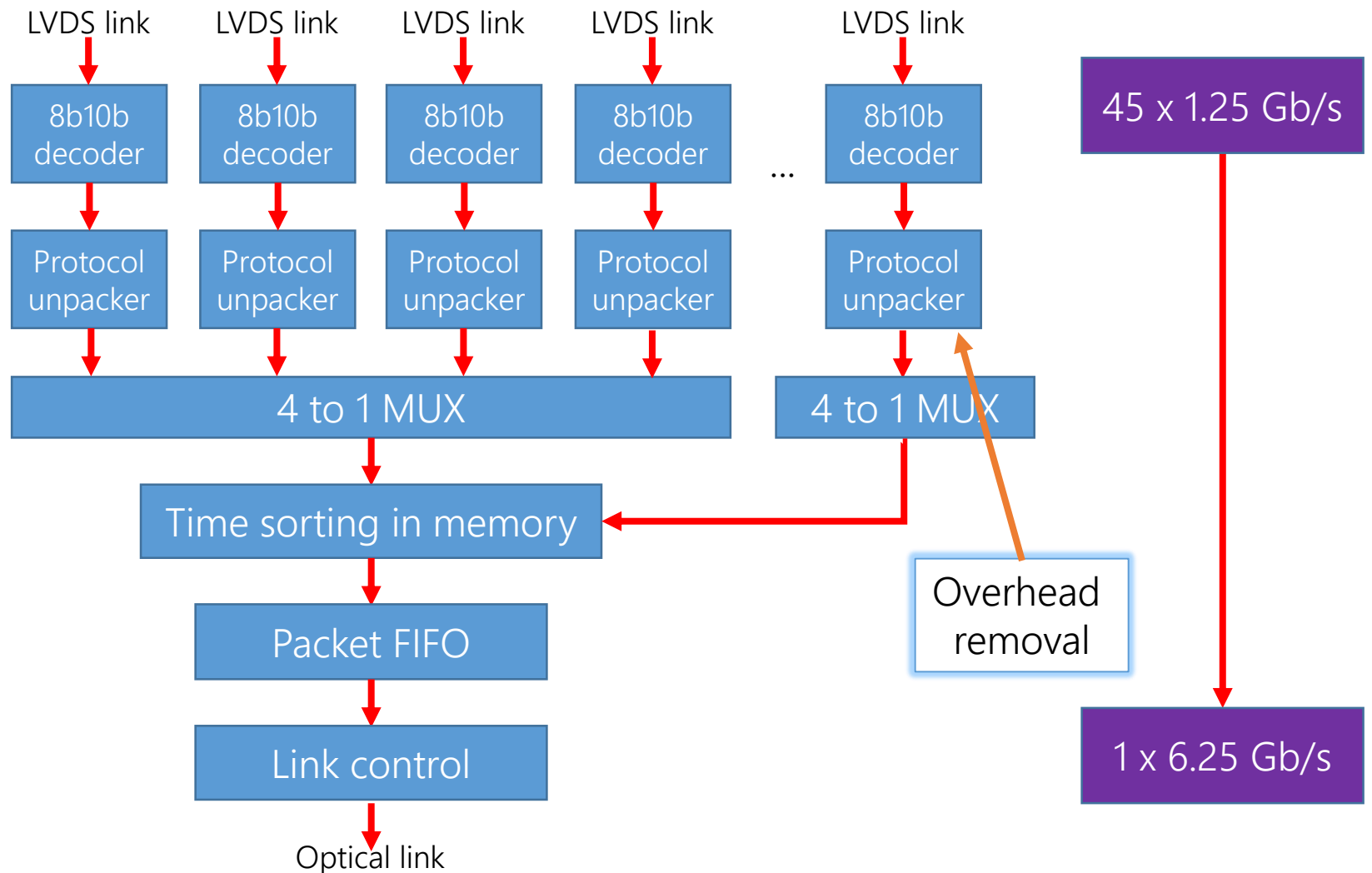
# Front-end Firmware Description





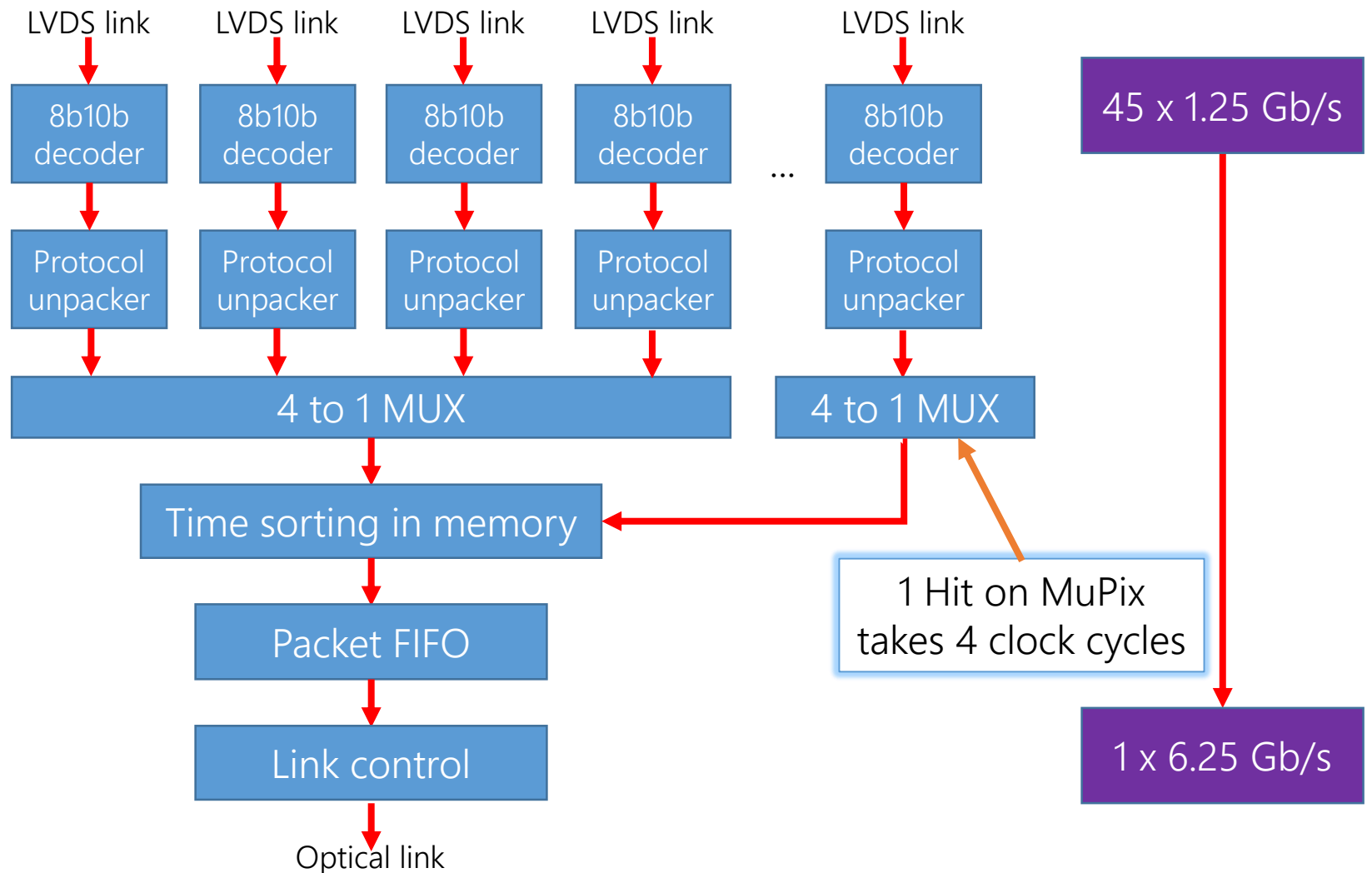


# Front-end Firmware Description



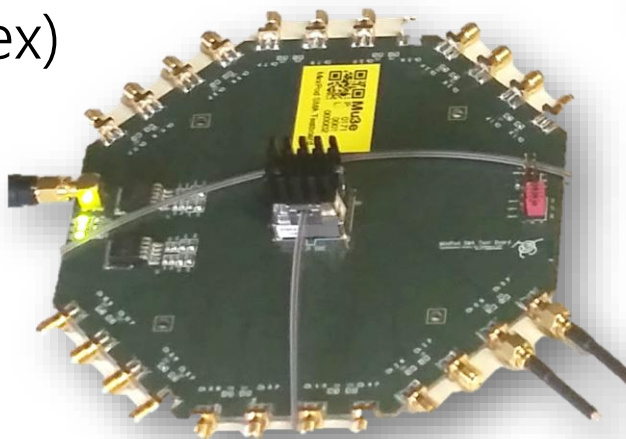
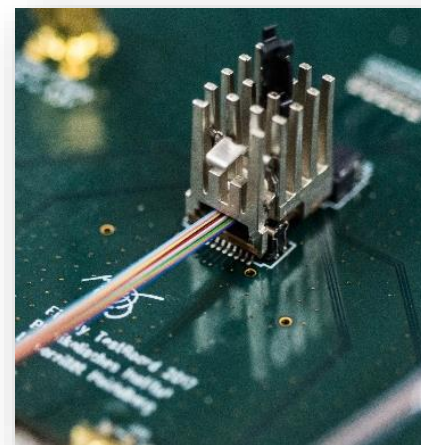


# Front-end Firmware Description



# Optical Components

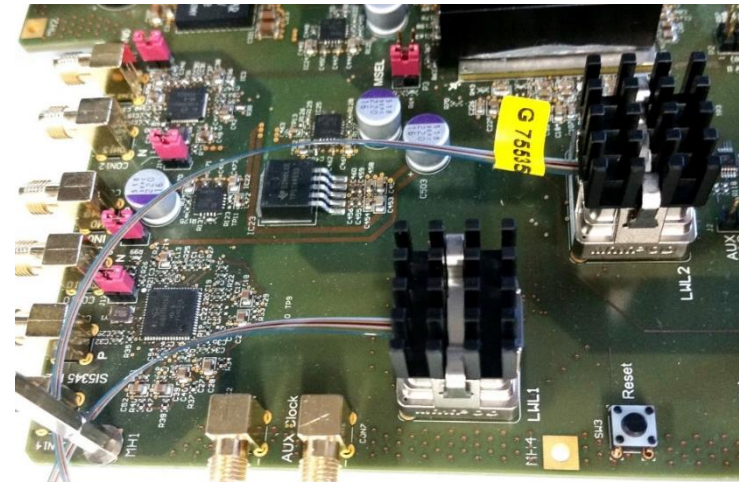
- All transceivers tested extensively
- Front-end & clock distribution:  
Samtec Firefly (x4 duplex, x12 simplex)  
also in magnetic field (0.6 T)
- Switching board:  
MiniPod (x12 simplex)
- Receiving card:  
QSFP (x4 duplex)



# Optical Data Transmission Tests

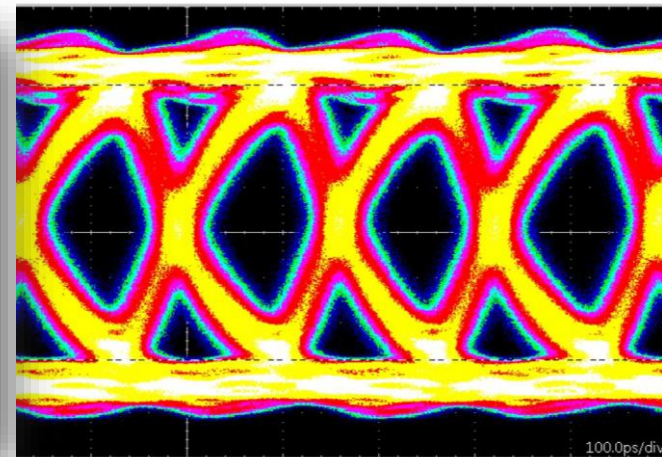
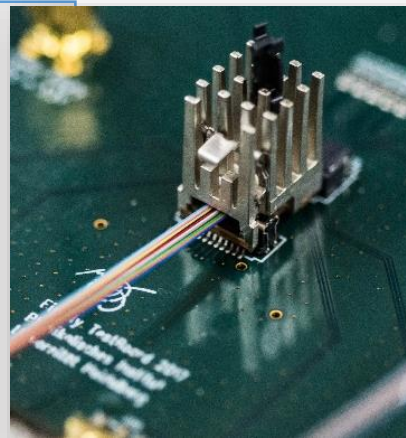
## Minipods

- 12-fold optical transmitter and receiver
- 1 m long multi mode fibre
- 12 channels at 6.25 Gb/s
- Error-free: BER <  $10^{-16}$



## Samtec Firefly

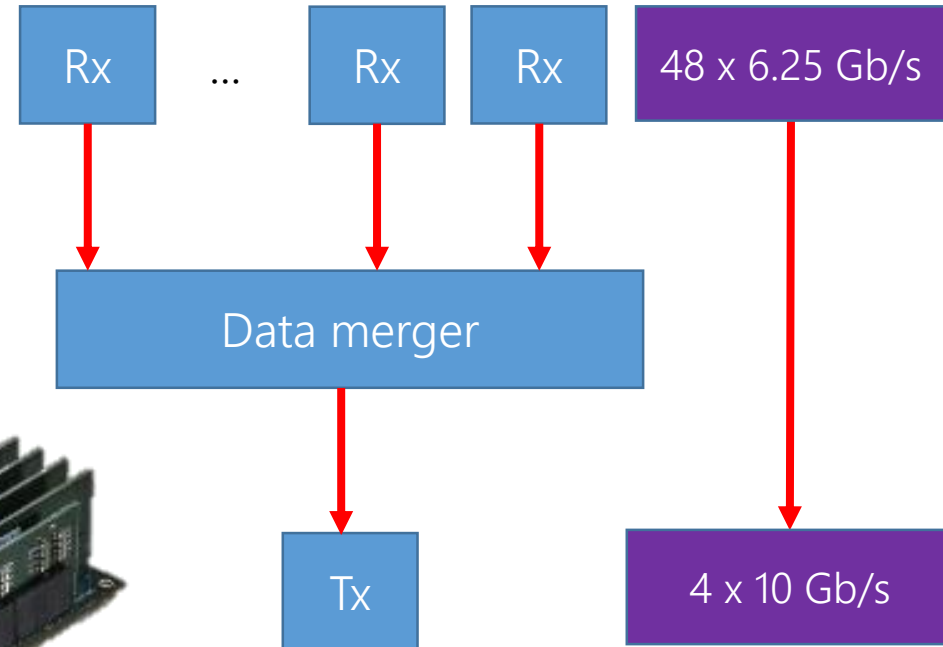
- 4-fold optical transceiver
- Tested setup:  
error free up to 8 Gbps
- BER <  $10^{-15}$



6 Gbps PRBS7 data after optical transmission with Samtec Firefly

# Switching Boards

- PCIe40 board (LHCb, ALICE)
- Arria10 FPGA
- 48 optical Tx and Rx
- 2 PCIe3 x8 interfaces
- Delivery in 2018/2019

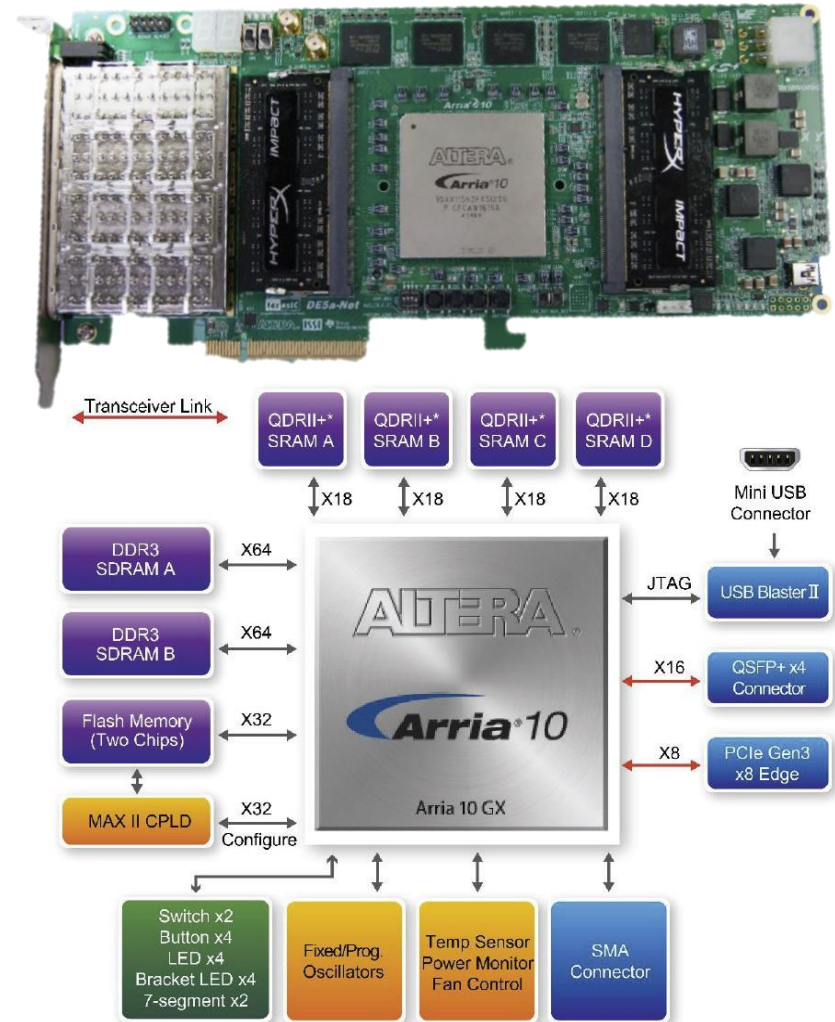






# GPU Farm: Receiving Card

- Commercial DE5a-NET board (Terasic)
- Large Arria10 FPGA
- Two banks of DDR3 memory
- PCIe 3.0 x8 interface
- 4 QSFP optical transceivers
- Daisy chain of optical links between PCs







# GPU Filter Farm

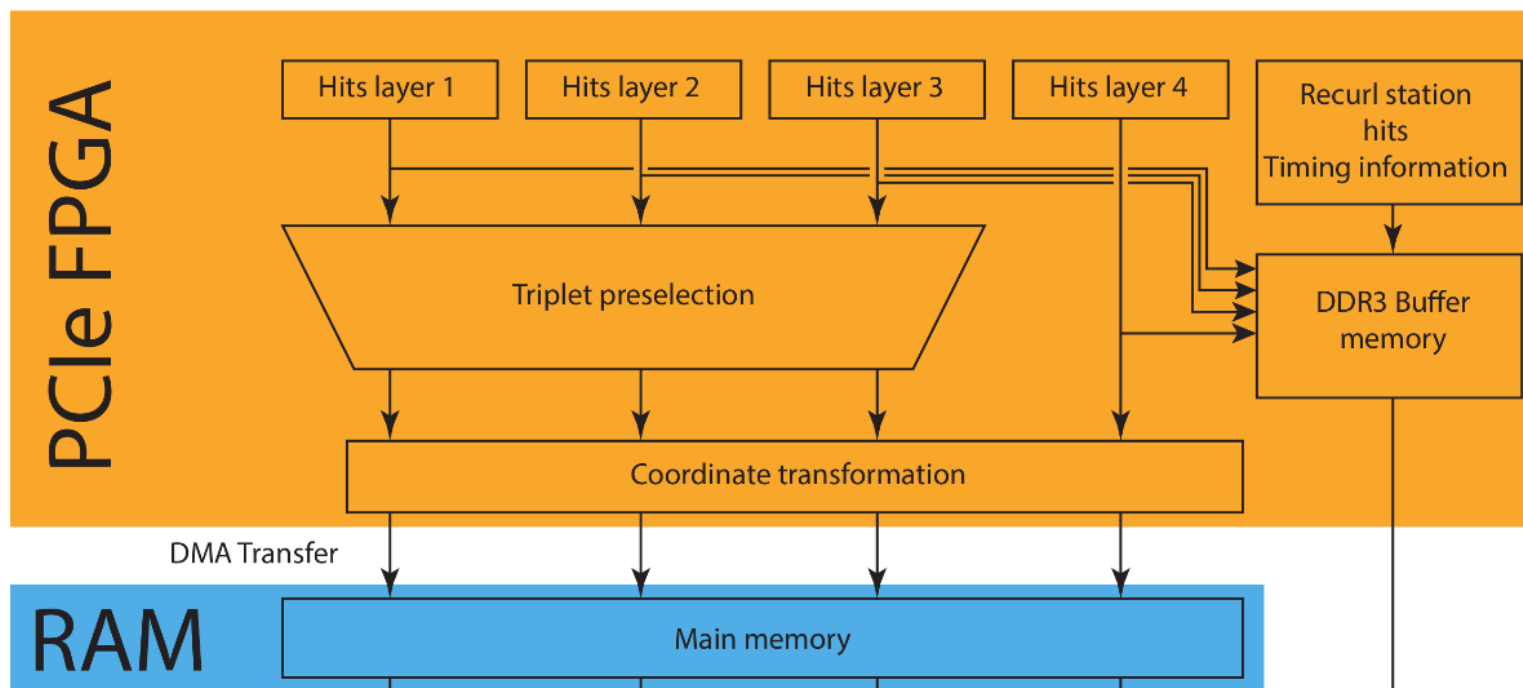
- Time slices of 50 ns for track & vertex search
  - Process  $20 \cdot 10^6$  time slices per second
- 12 filter farm PCs with one GPU each
- Process at least  $1.7 \cdot 10^6$  time slices per second
  - **GPUs are ideal for this task!**
- Thousands of cores
- Optimal parallel performance
- Best suited for many floating-point operations / second





# GPU Event Filtering

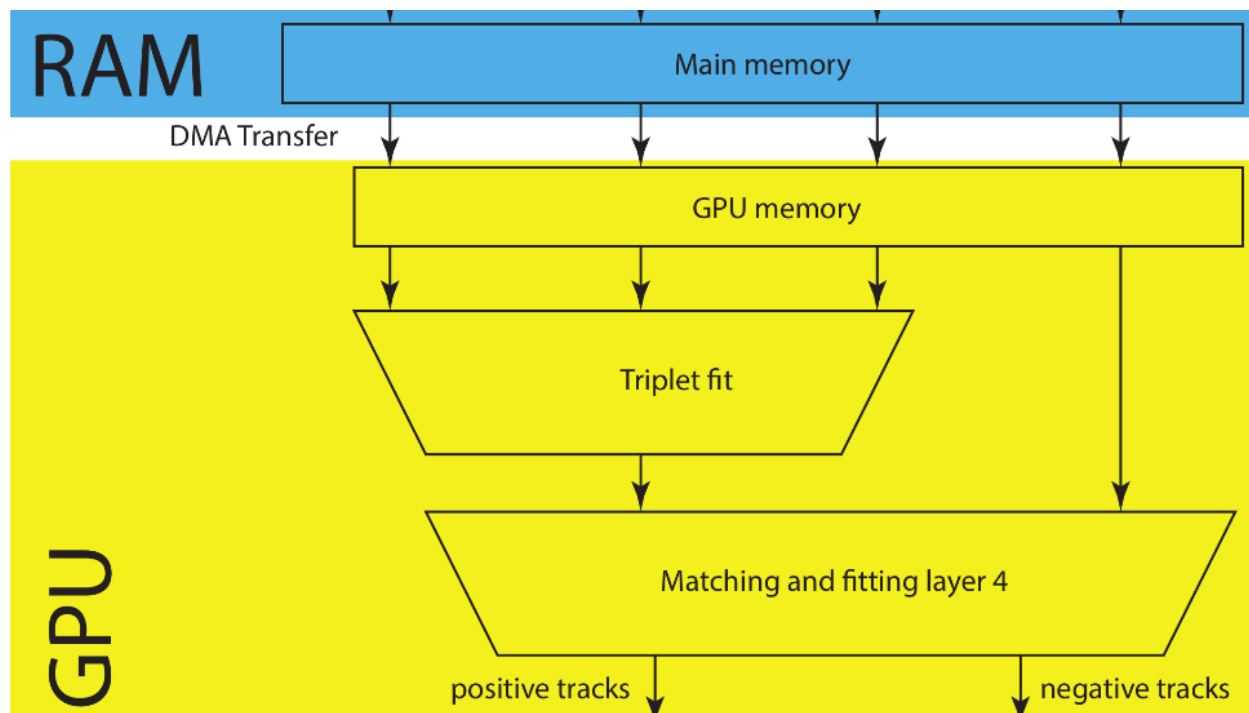
- On-FPGA: Track preselection using geometrical criteria
- Coordinate transformation
- Direct memory access to PC memory





# GPU Event Filtering

- Direct memory access to GPU memory
- Track fitting: *Triplet Fit* [arXiv:1606.04990](https://arxiv.org/abs/1606.04990)  
Multiple scattering dominated, linearized, can be parallelized





# GPU Event Filtering

- o Vertex selection for signal topology:  $2 e^+ + 1 e^-$

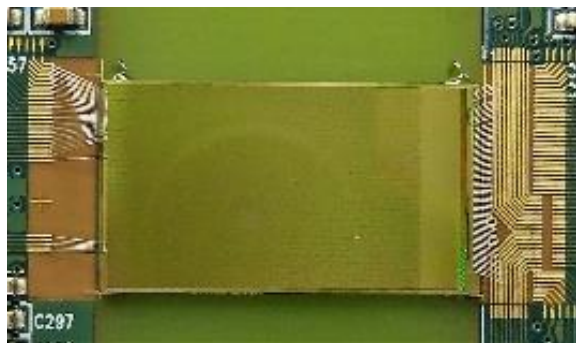


# GPU Event Filtering

- o Vertex selection for signal topology:  $2 e^+ + 1 e^-$

Implementation test on GTX 1080 Ti  
 $2.0 \cdot 10^6$  time slices processed  
> required  $1.7 \cdot 10^6$

# Mu3e Pixel Readout Demonstrator



Pixel sensors  
Large prototype: MuPix8  
*operational*

Front-end FPGA  
Prototype boards: Stratix IV  
*operational*

Switching board  
PCIe40 (LHCb development)  
*delivery 2018*

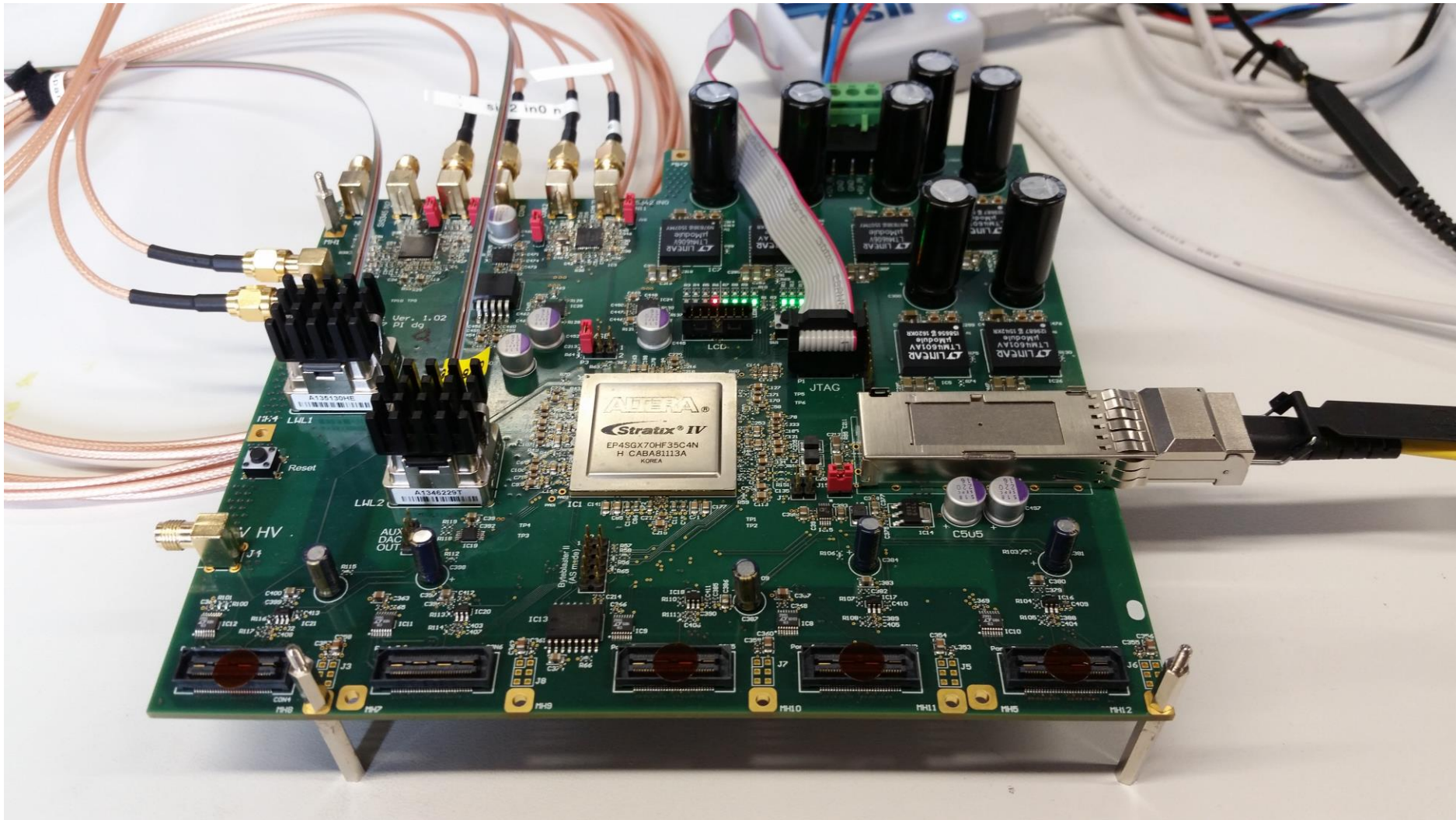
PC  
FPGA on PCIe card: Stratix IV





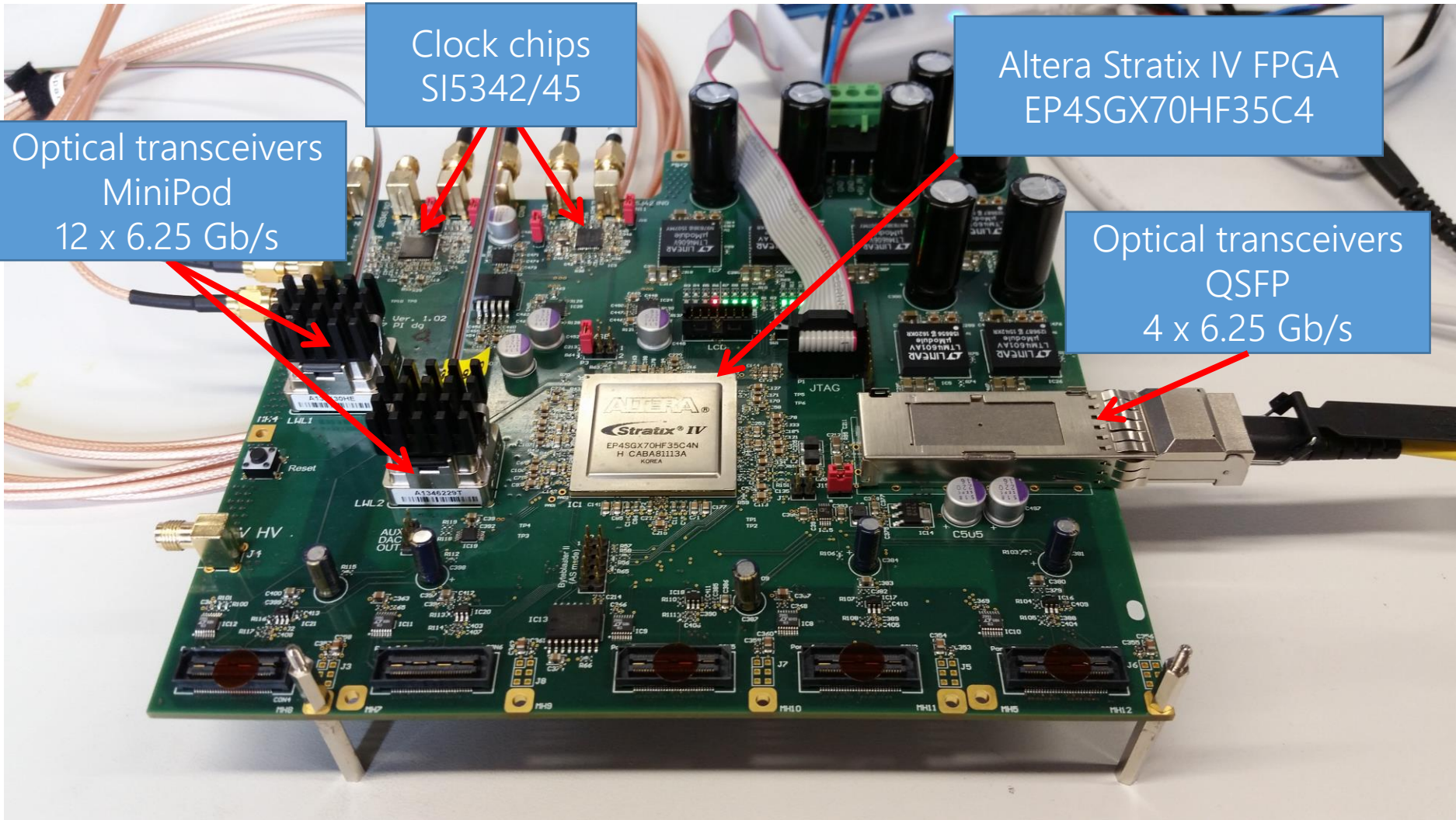


# Mu3e Front-End Board Prototype





# Mu3e Front-End Board Prototype



Optical transceivers  
MiniPod  
12 x 6.25 Gb/s

Clock chips  
SI5342/45

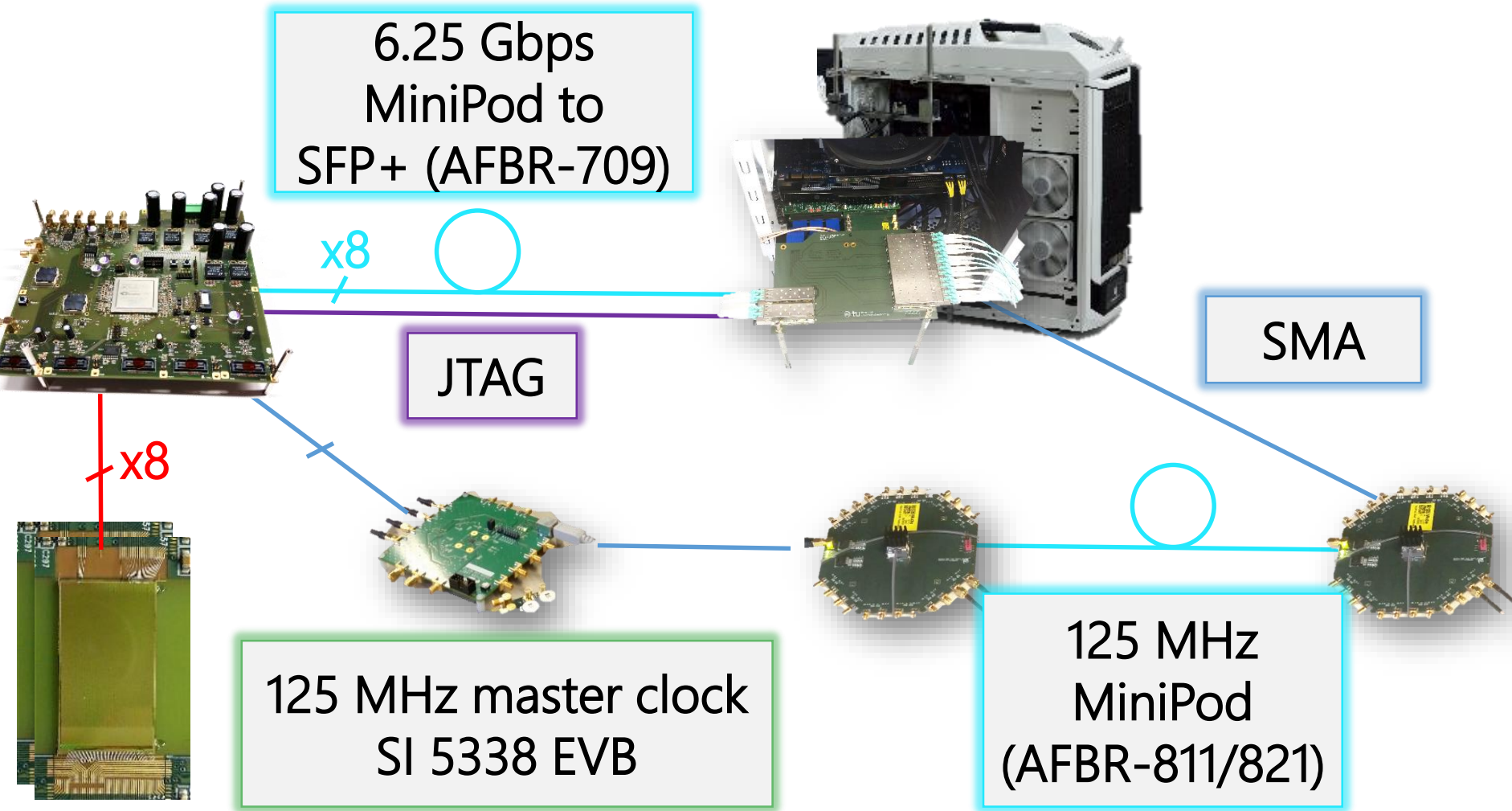
Altera Stratix IV FPGA  
EP4SGX70HF35C4

Optical transceivers  
QSFP  
4 x 6.25 Gb/s





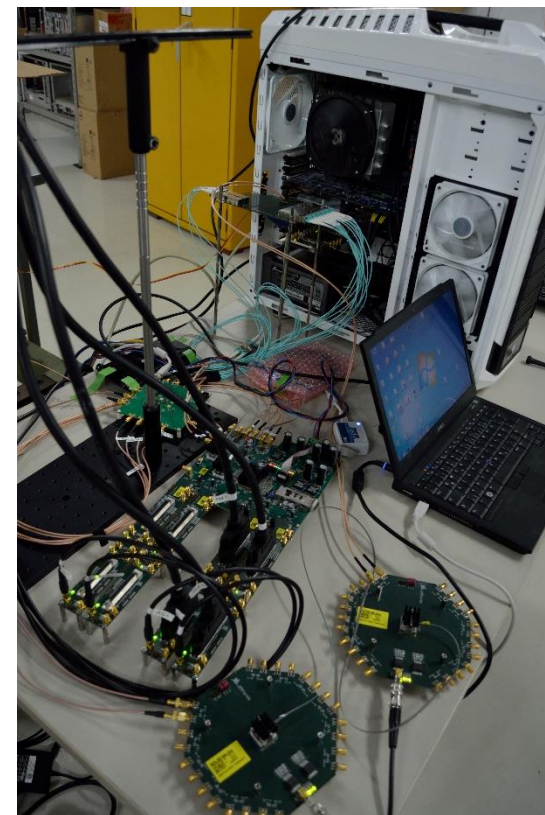
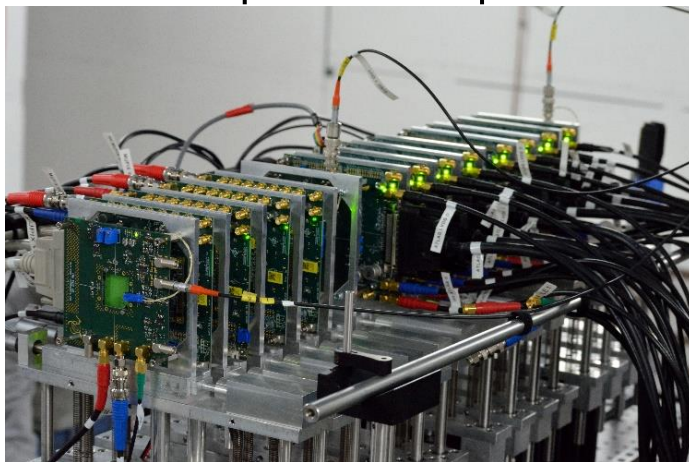
# Optical and Electrical Connections



# Hardware Operational Tests

Successful operation of eight MuPix8 in parallel on a test beam at DESY

- Configuration of sensors ✓
- Data transmission:
  - Sensors to front-end ✓
  - Front- to back-end ✓
- Sensors respond to positron beam ✓





# Summary

- Mu3e sensitivity goal requires high statistics
- Trigger-less DAQ
- Three FPGA-based DAQ layers
- All subsystems run synchronously
- Data reduction:  
From 3.8 Tb/s raw data to < 100 MB/s to disk
- Demonstrator readout tests successful

