

Advanced Digital Pulse Processing applied to Monolithic Segmented Detectors for Spectroscopy



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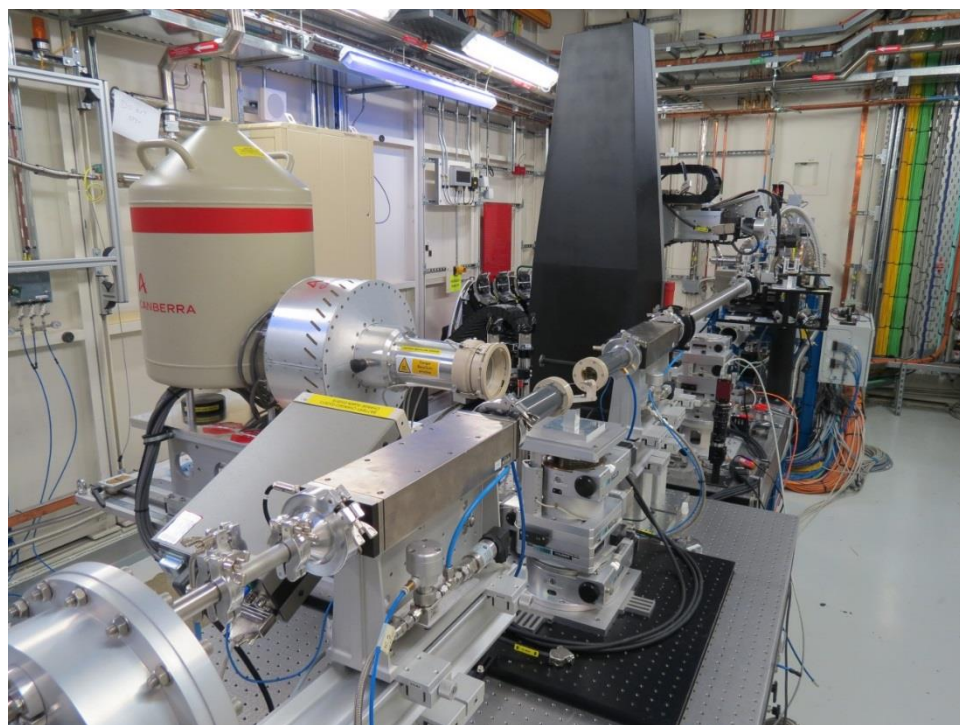
² Science & Technology Facilities Council (STFC), Daresbury Laboratory, Warrington, Cheshire, UK

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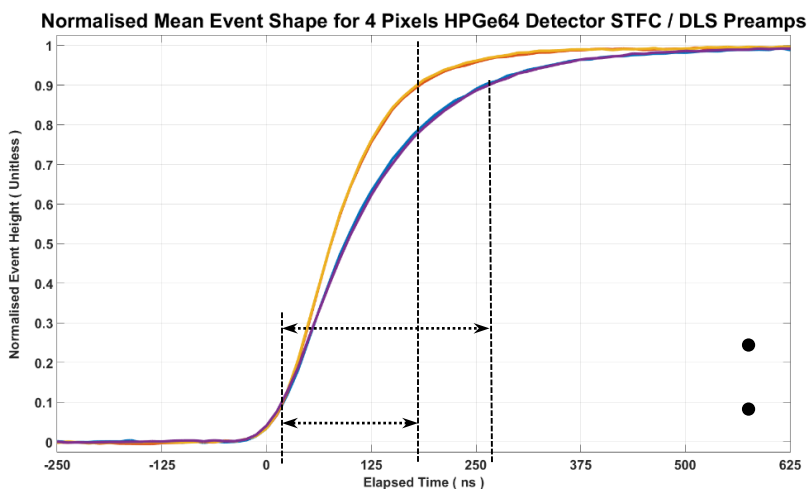
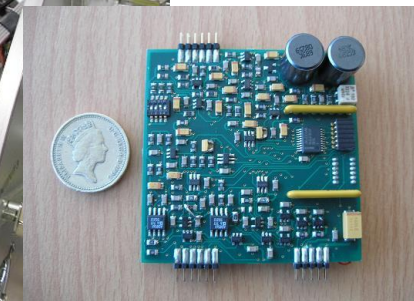
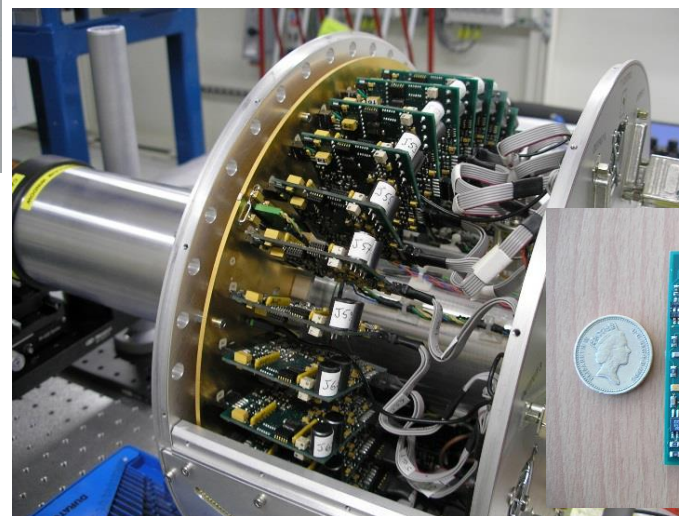
Graham Dennis – DLS Detector Group



Beam Line I20-Scanning : Fluorescence XAS Detector



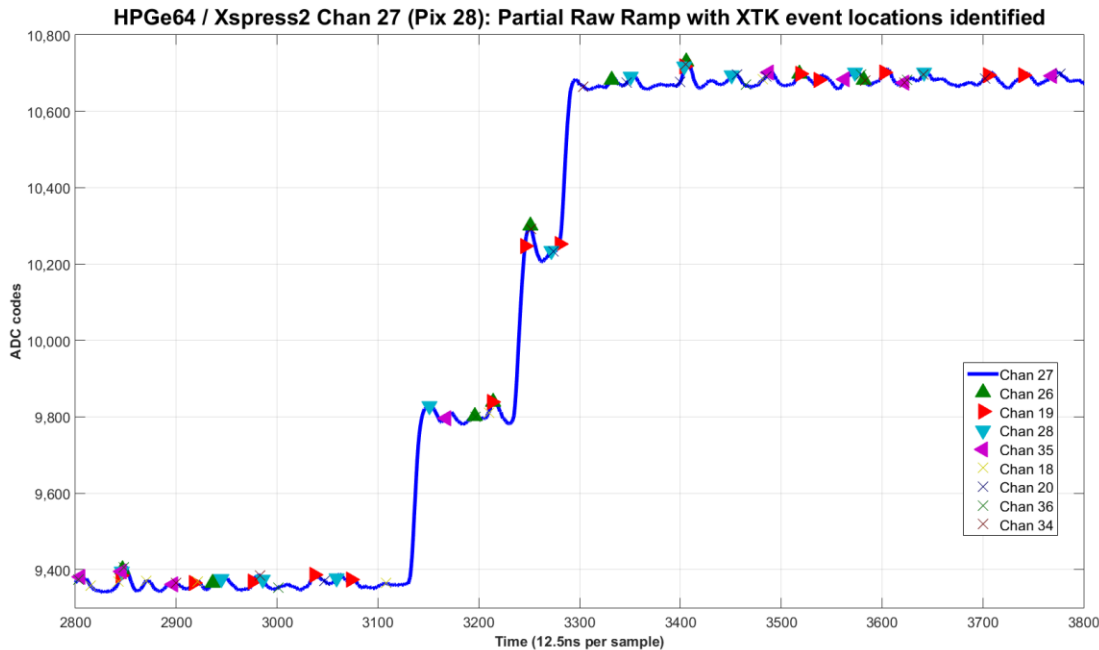
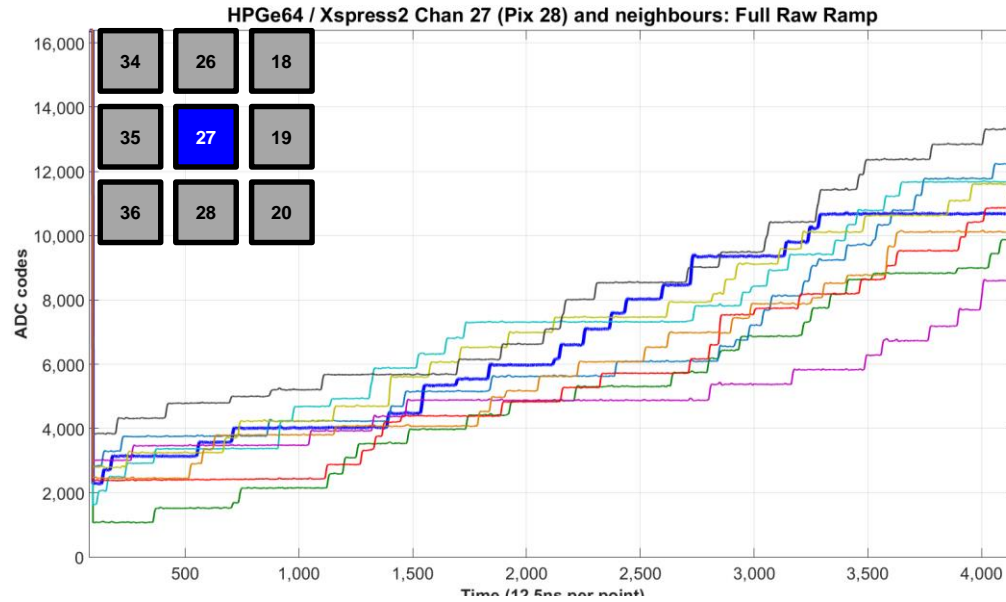
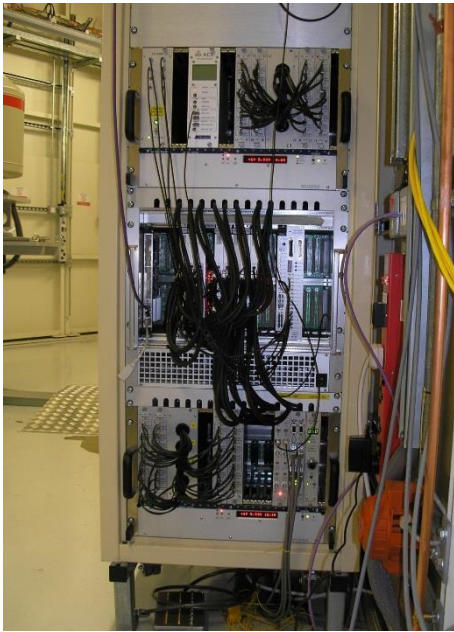
- Challenging samples
4 keV – 20(40) keV
- Canberra **HPGe64** (2009 vintage) ...
- Segmented 8 x 8 matrix...each
pixel 5mm x 5mm
- Mask (retro)fitted
- Global Reset mode



- STFC TrRst CSA (JFET + discrete)
- $T_{\text{rise10-90}} : 164\text{ns} \text{ \& \ } 245\text{ns}$

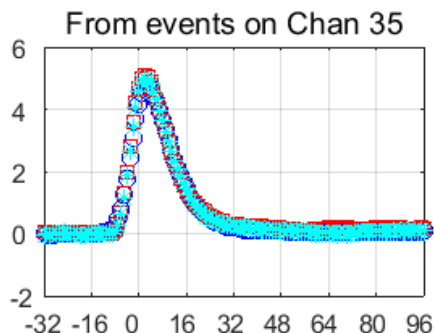
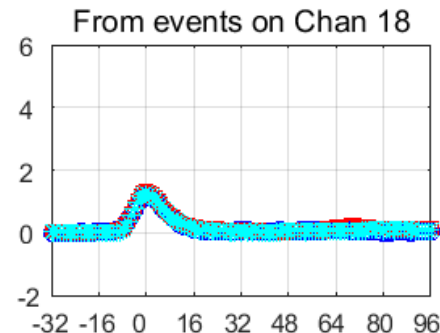
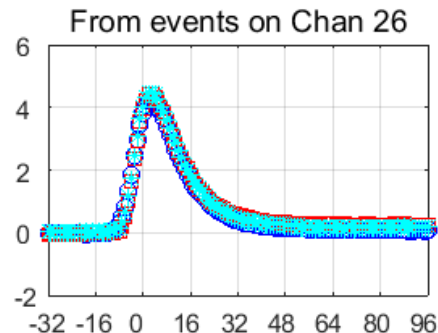
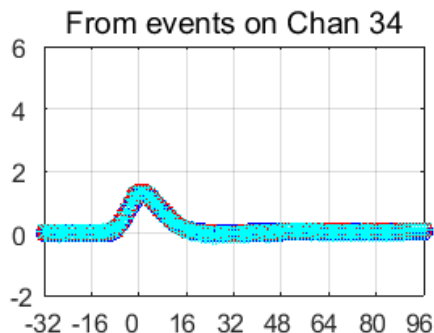


...Xspress 2 DPP & measurement of Event Crosstalk (XTK)



- STFC Xspress 2 DPP
- Resolution poor for CR>200 kcps per pixel
- “Noise” on raw signals correlates with Event XTK from neighbour pixels...

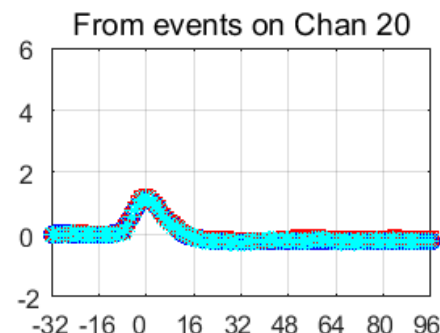
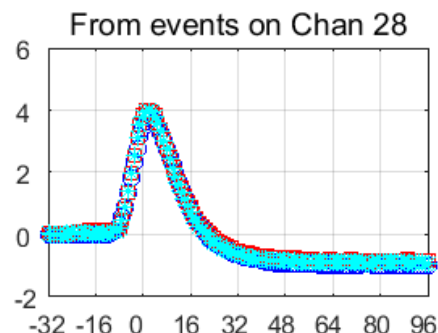
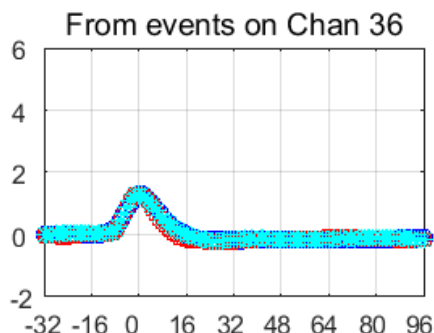
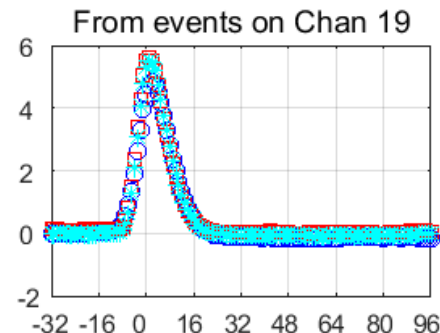
HPGe64: Typical Event XTK from neighbour pixels



**Normalised Xtalk on
Victim Chan 27**

(Mn red, Zn cyan & Mo blue)

X: Sample num rel. ZeroX
Y: Percent of Neighbour Engy

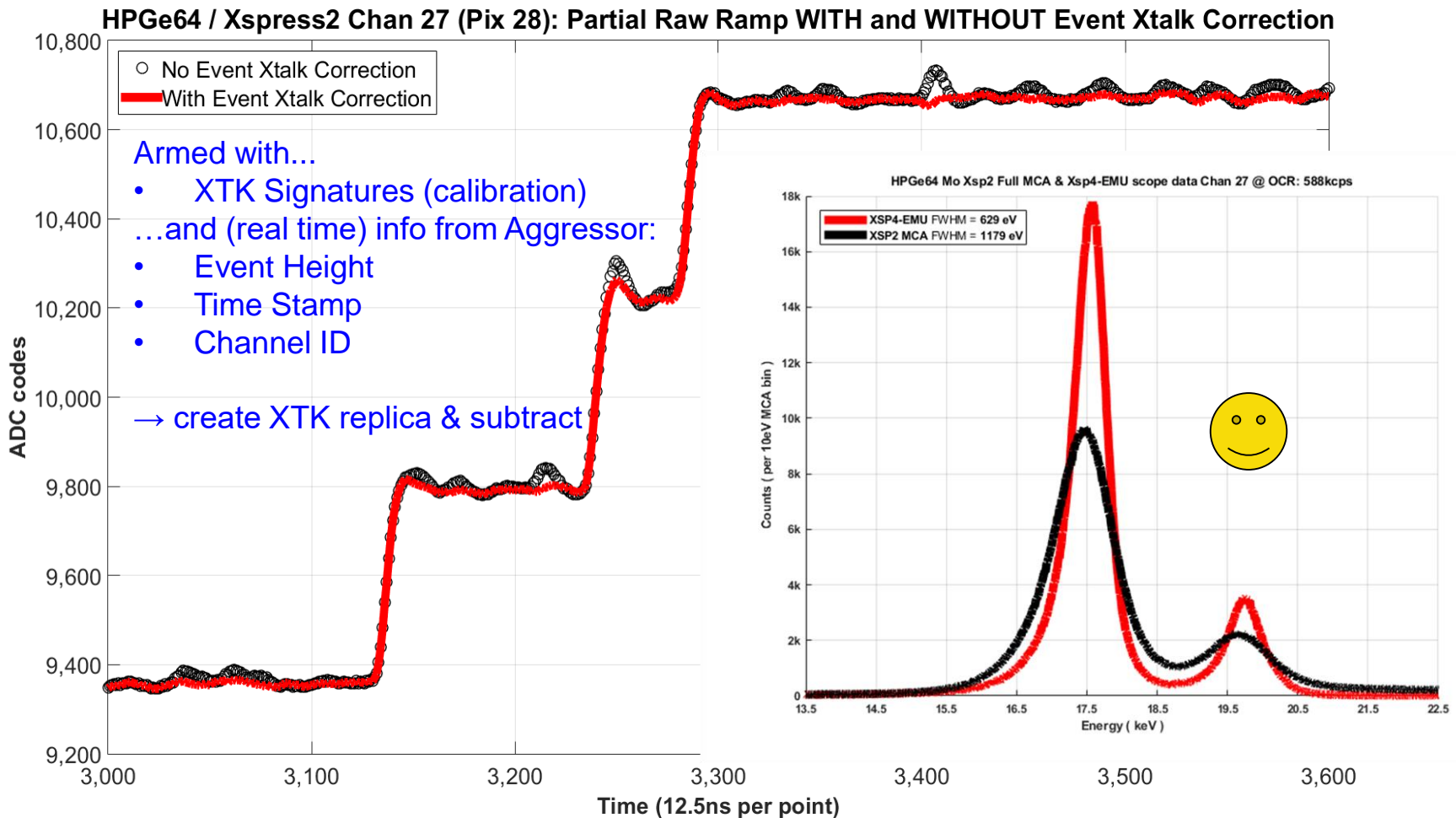


X-axis time: $-0.4\mu\text{s} \leq T_{\text{event}} \leq +1.2\mu\text{s}$

Y-axis percentage energy imparted from aggressor to victim channel



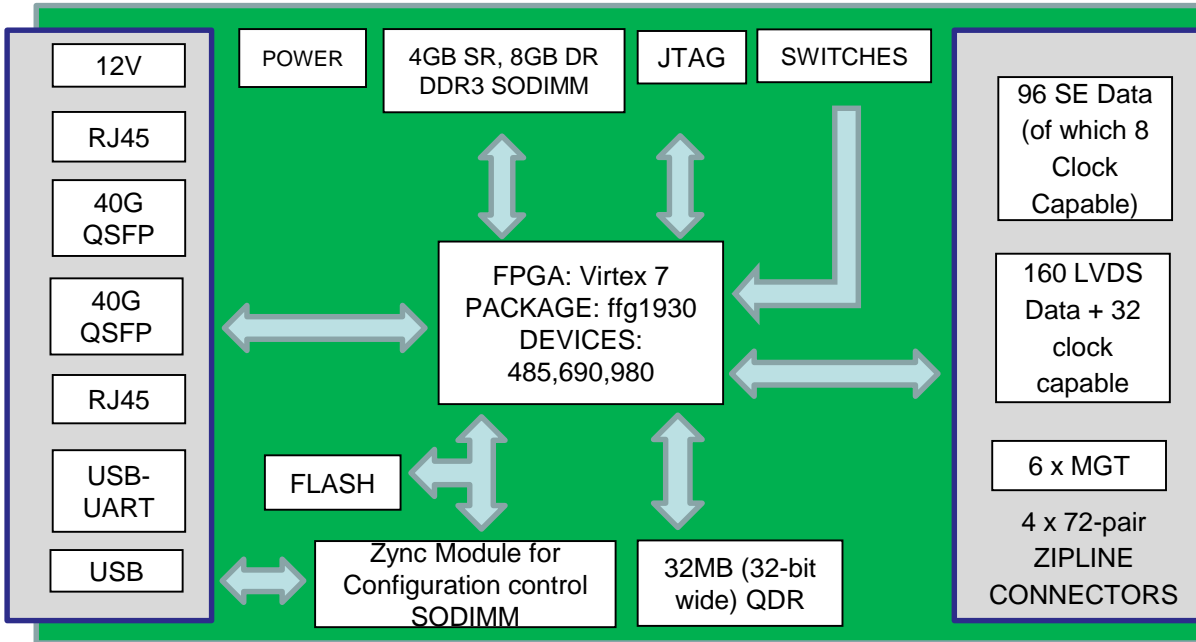
HPGe64: Raw event signal w/wo XTK Correction



...but requires larger FPGA, synchronous sampling,
and real time chan-to-chan communication

...justification for new DPP...Xspress 4

Xspress 4 Hardware (1): FEM-2 (Custom generic FPGA Module)



Xspress 4 requirements

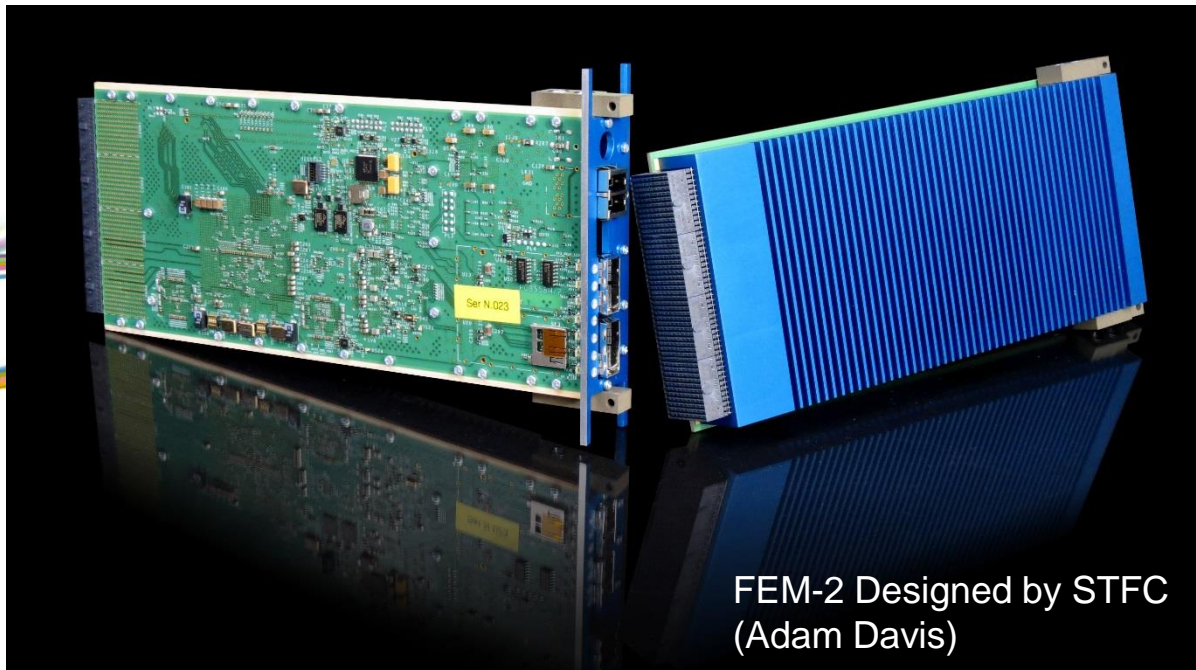
- **Virtex7-690**
- 4GB memory
- Enclustra MarsZX3 Zync SoC

Edge-Connector IO

- **192 LVDS pairs IO**
- **96 SE**
- **6 x MGT ($\leq 10\text{Gbs}$)**

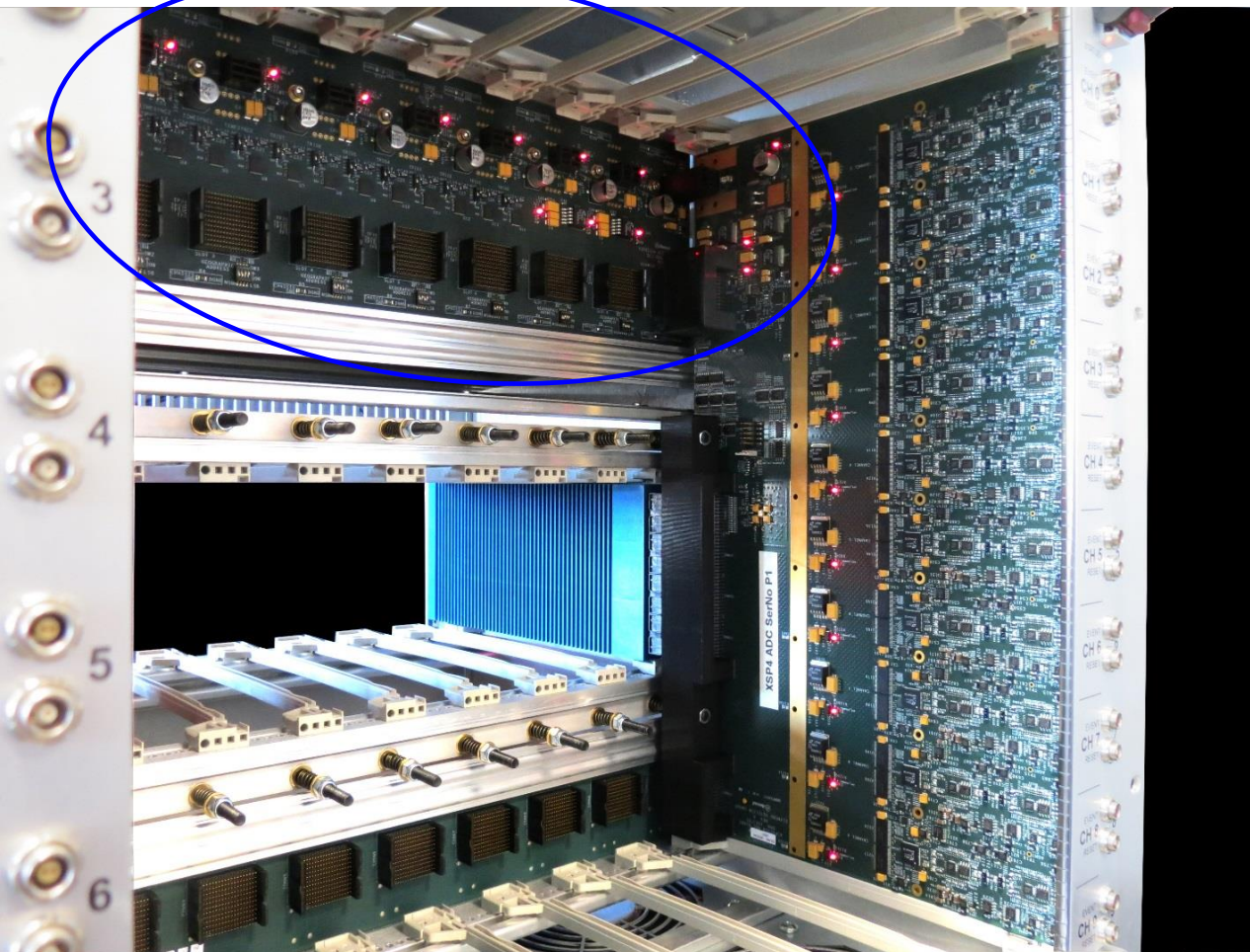
Xspress 4 External IO

- $\frac{1}{4}$ QSFP fibre-optic (@10Gbs UDP)
- 1GigE copper



FEM-2 Designed by STFC
(Adam Davis)

Xspress 4 Hardware (2): ADC Board & Active Midplane



ADC Board

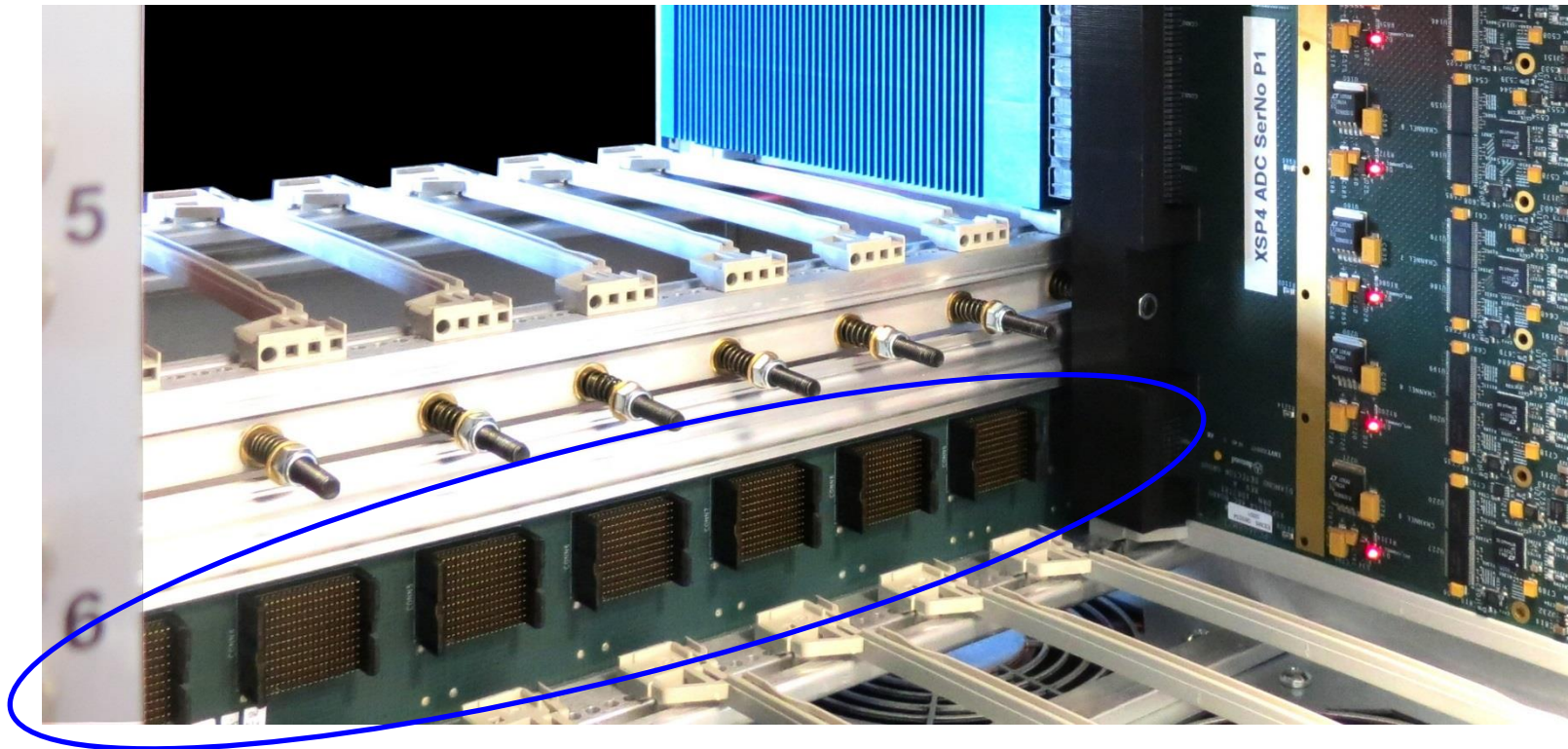
- 10 channel PCB
- Diff / SE Signal Input
- SE Reset Input
- S/W programmable gain / offset
- ADC 16bit @ 100MHz

Active Midplane

- 10 slots wide
- Ultra-low jitter Master Clock
- Very low skew Radial Triggers
- + others



Xspress 4 Hardware (3): Passive Midplane



FEM-2
Slot n-2

FEM-2
Slot n-1

FEM-2
Slot n

FEM-2
Slot n+1

FEM-2
Slot n+2

SATA

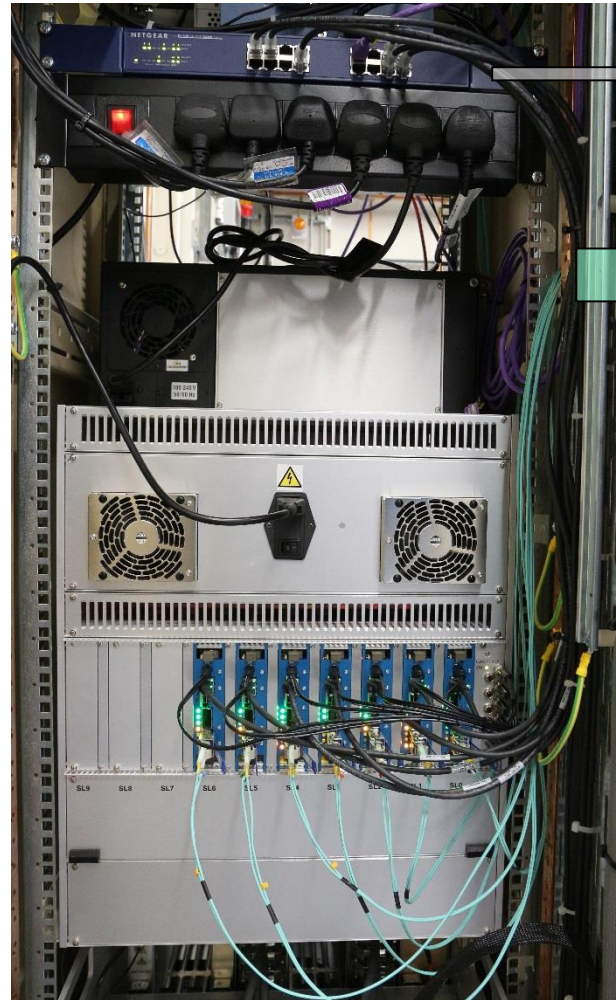
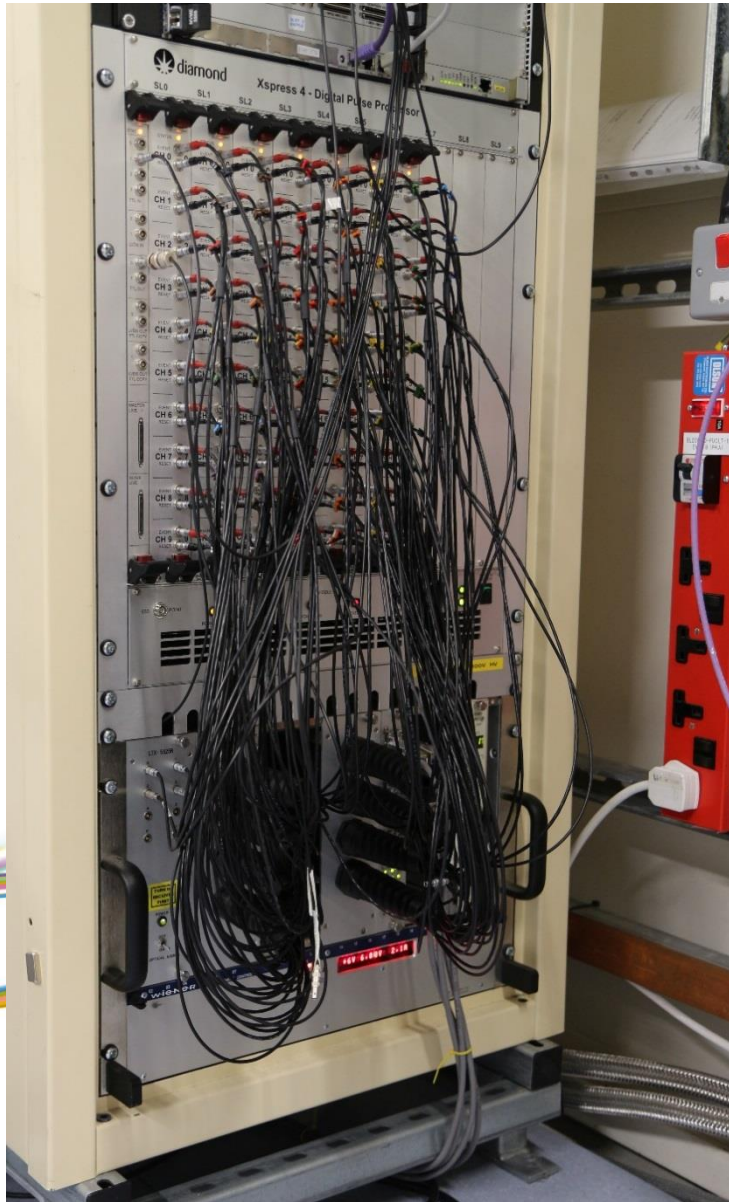
SATA

Passive Midplane

- Pnt-2-Pnt hi speed serial links
- Xsp4 – 3.125Gbs (64b/66b)



Xspress 4 Hardware On I20-Scanning



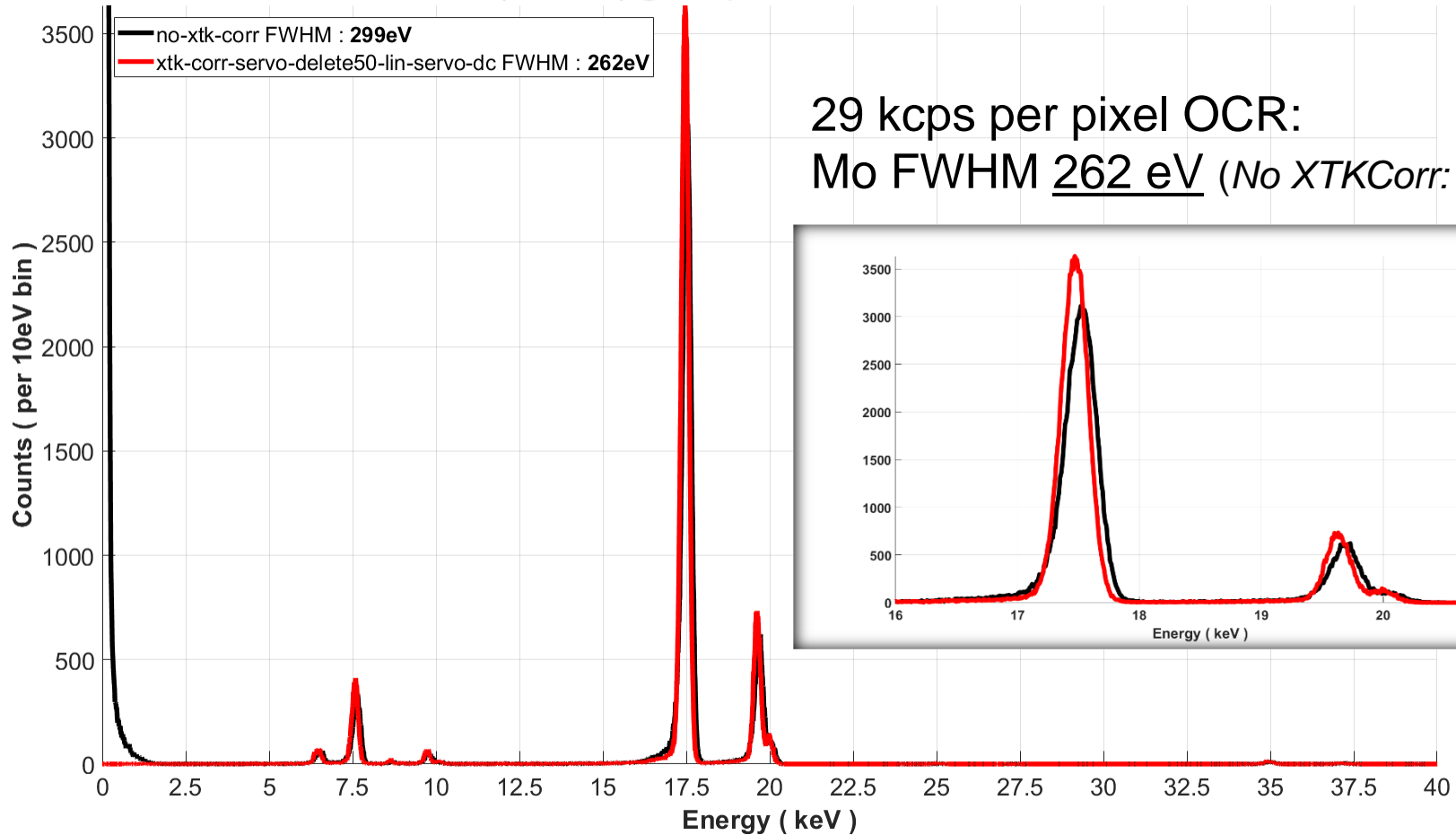
- 7 x 10Gbs UDP fibre optic
- 1 x 1GigE copper

Server access via SSH, EPICS & GDA

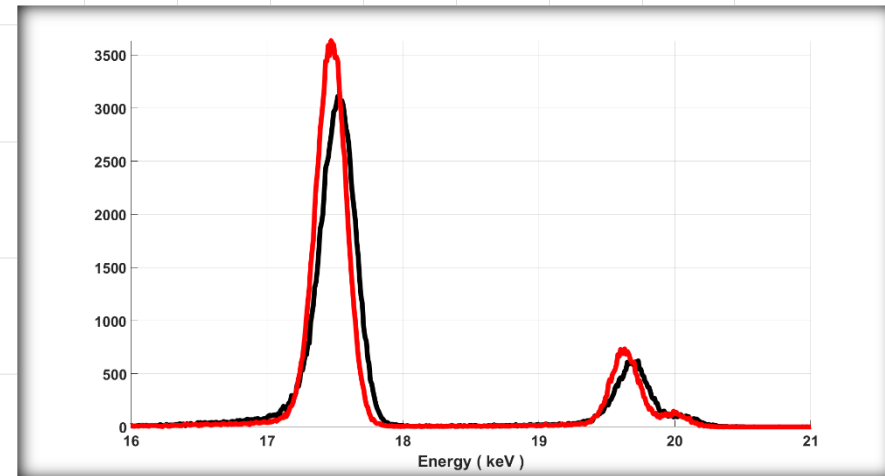


HPGe64 + Xspress 4 On I20-Scanning: Mo low rate

MCA Mo (17.47keV) @ 29kcps OCR HPGe64 + XSP4 : Chan 10

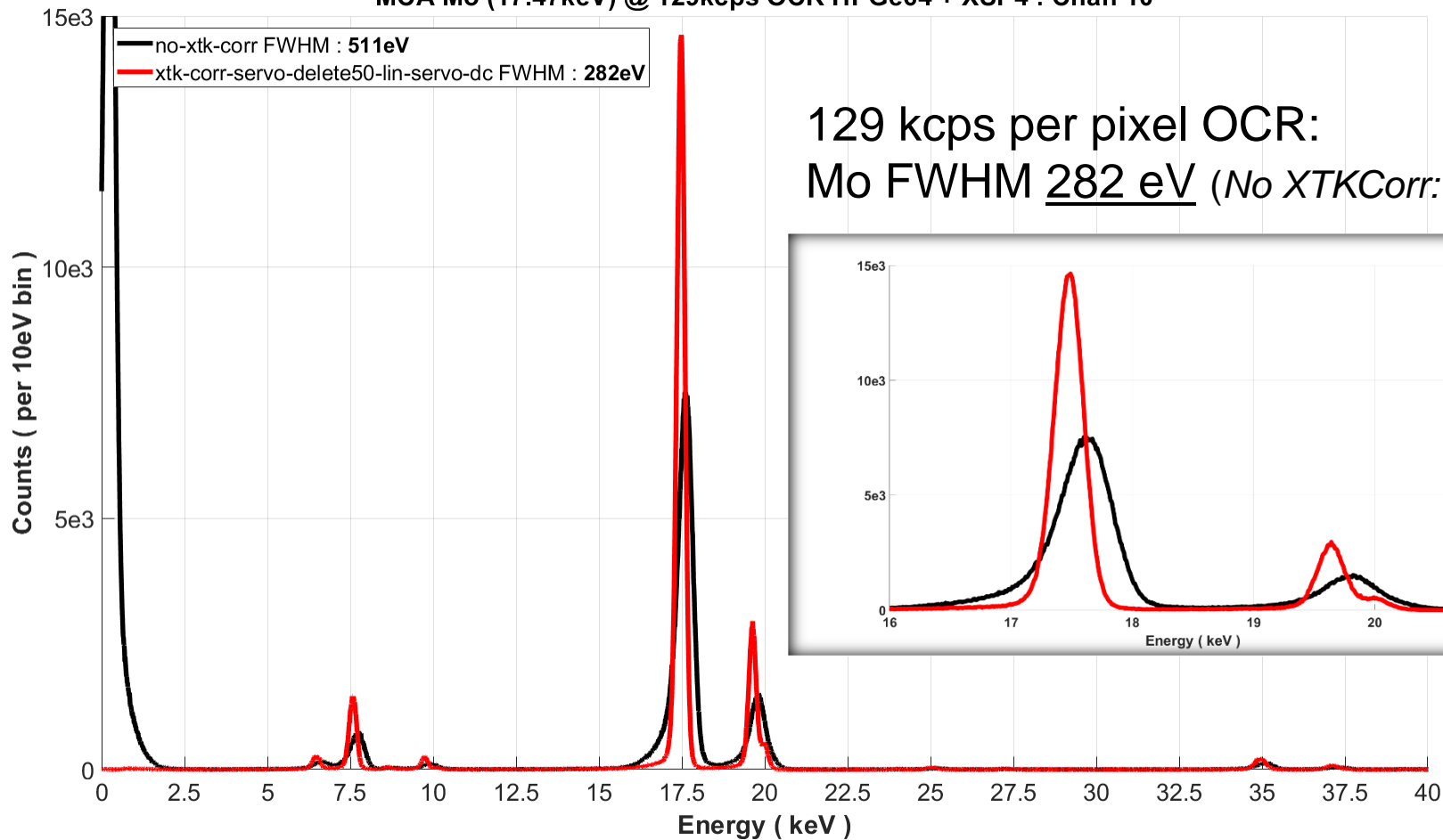


29 kcps per pixel OCR:
Mo FWHM 262 eV (No XTKCorr: 299 eV)

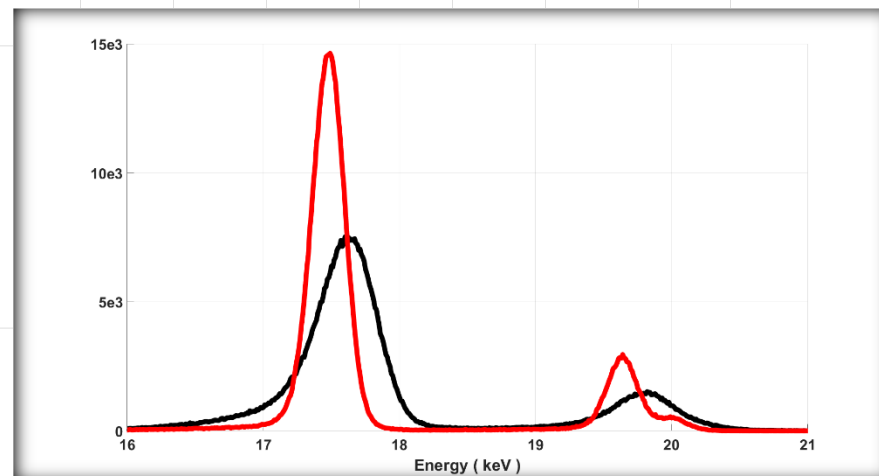


Mo medium-low rate

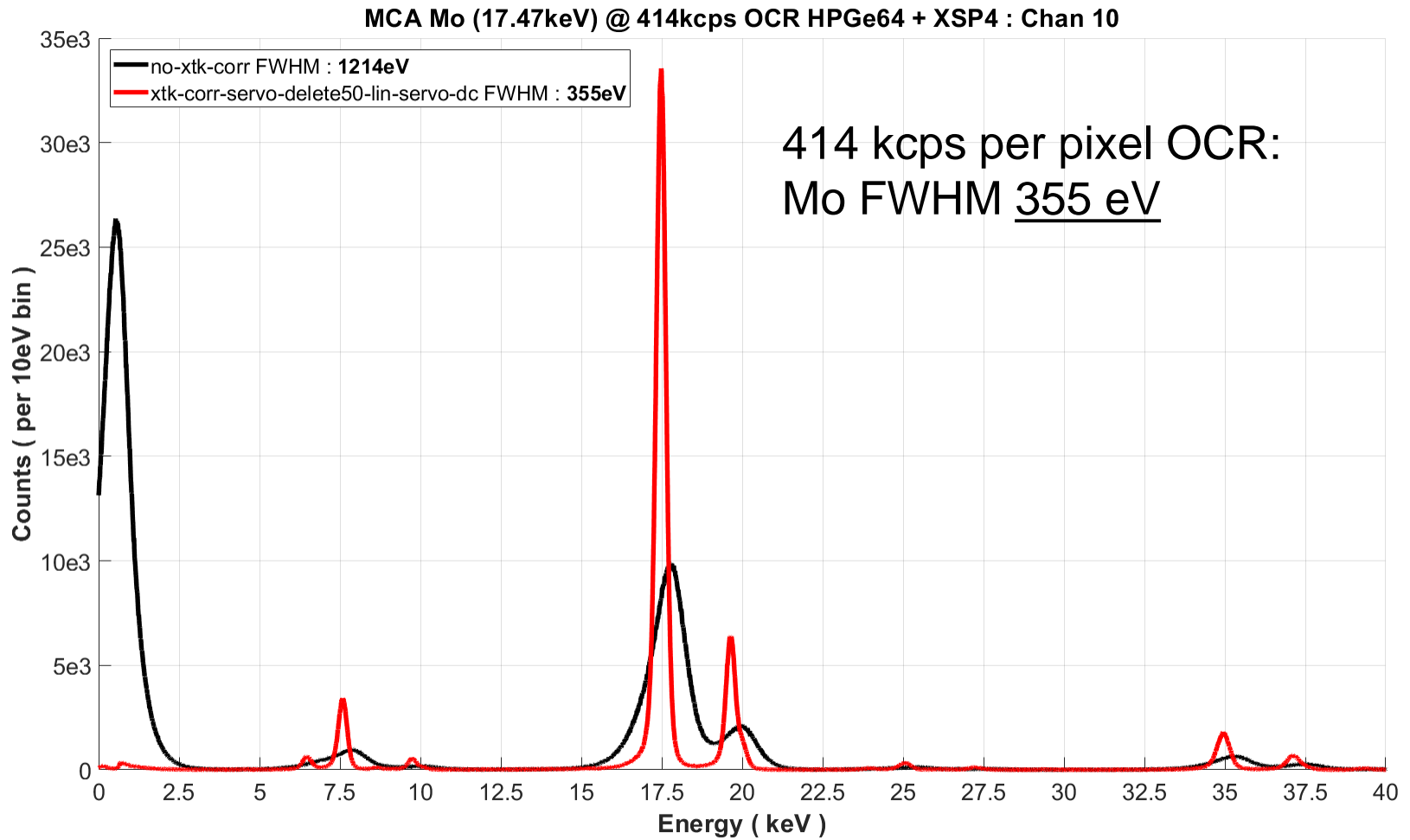
MCA Mo (17.47keV) @ 129kcps OCR HPGe64 + XSP4 : Chan 10



129 kcps per pixel OCR:
Mo FWHM 282 eV (No XTKCorr: 511 eV)

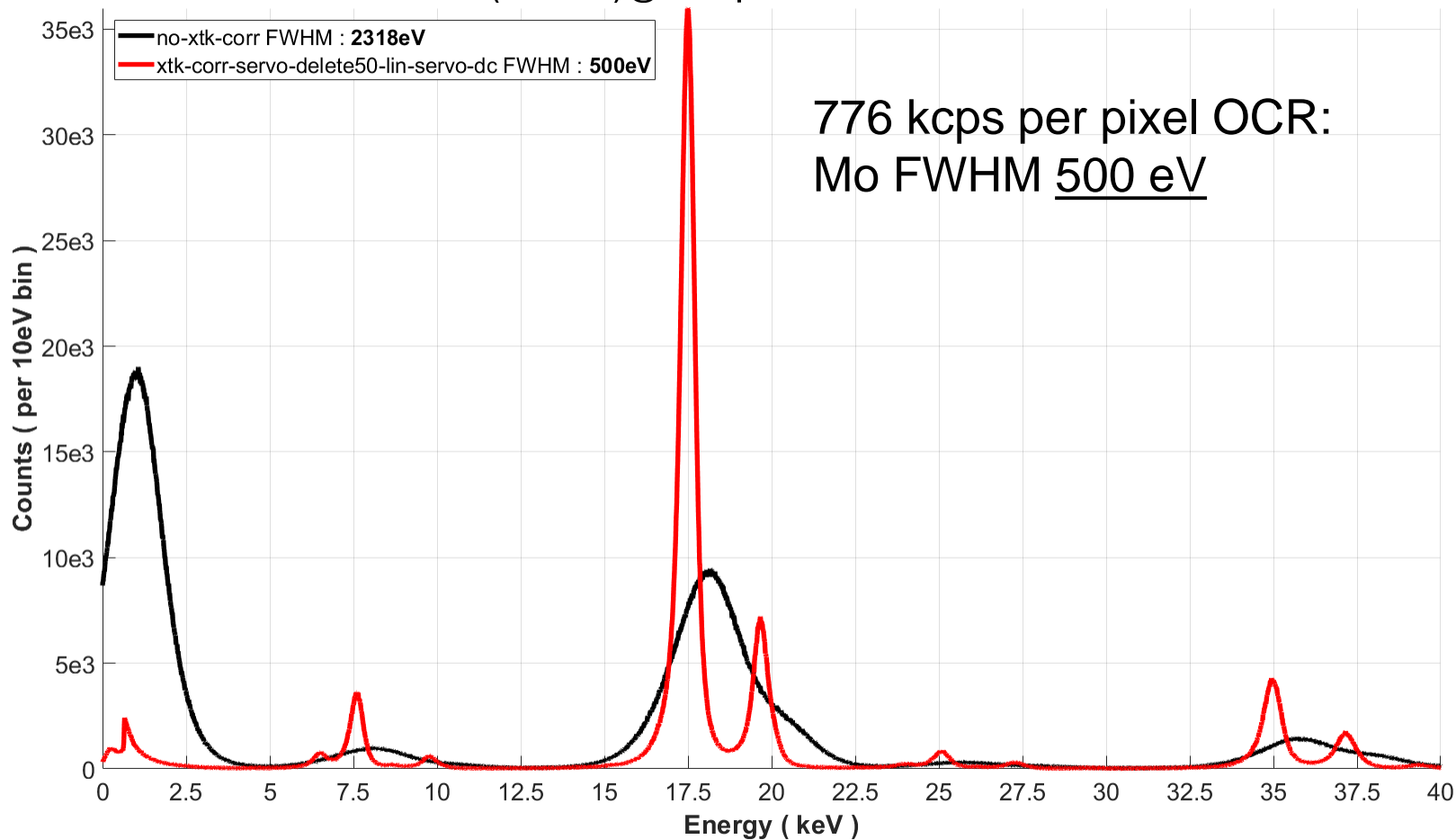


Mo medium rate

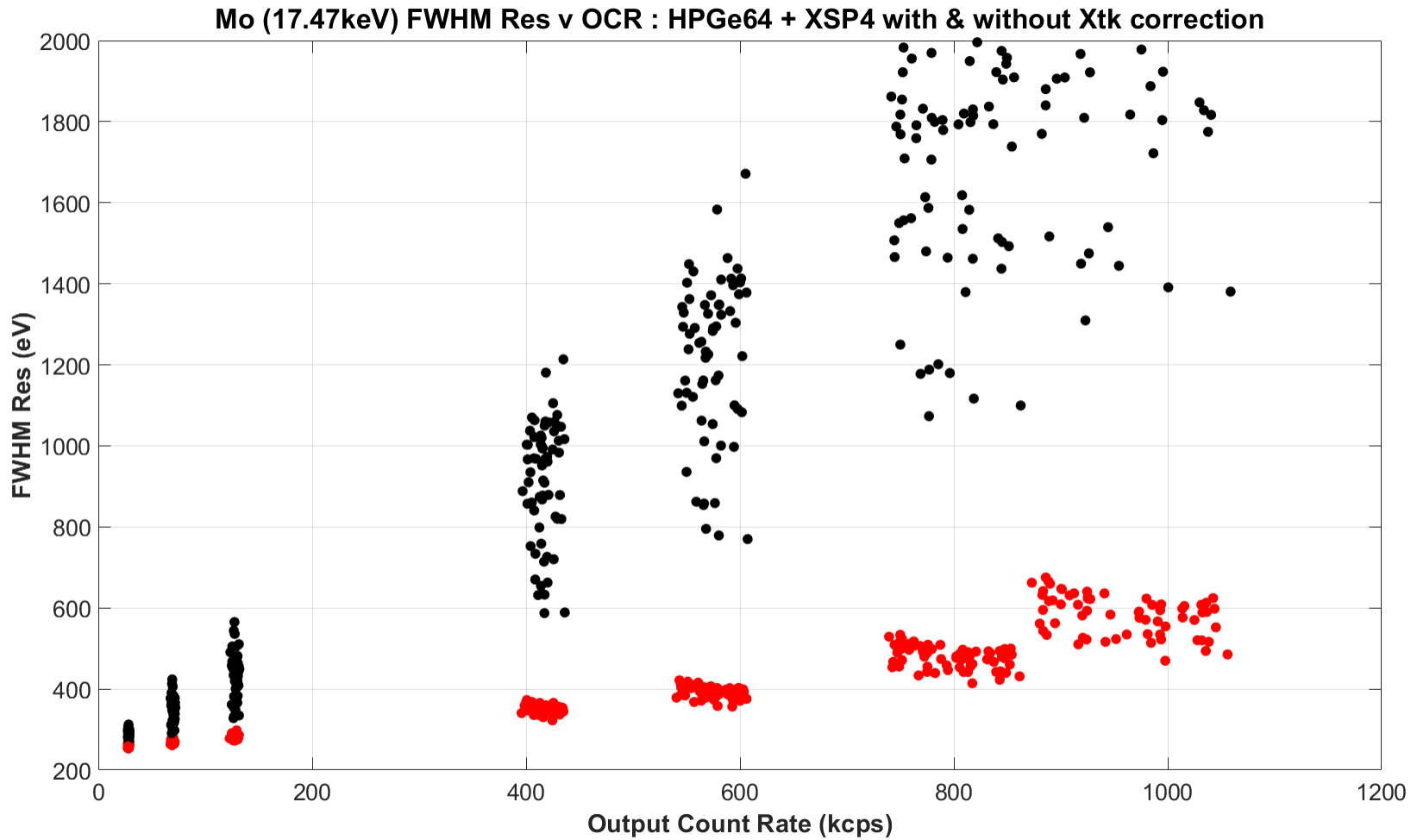


Mo high rate

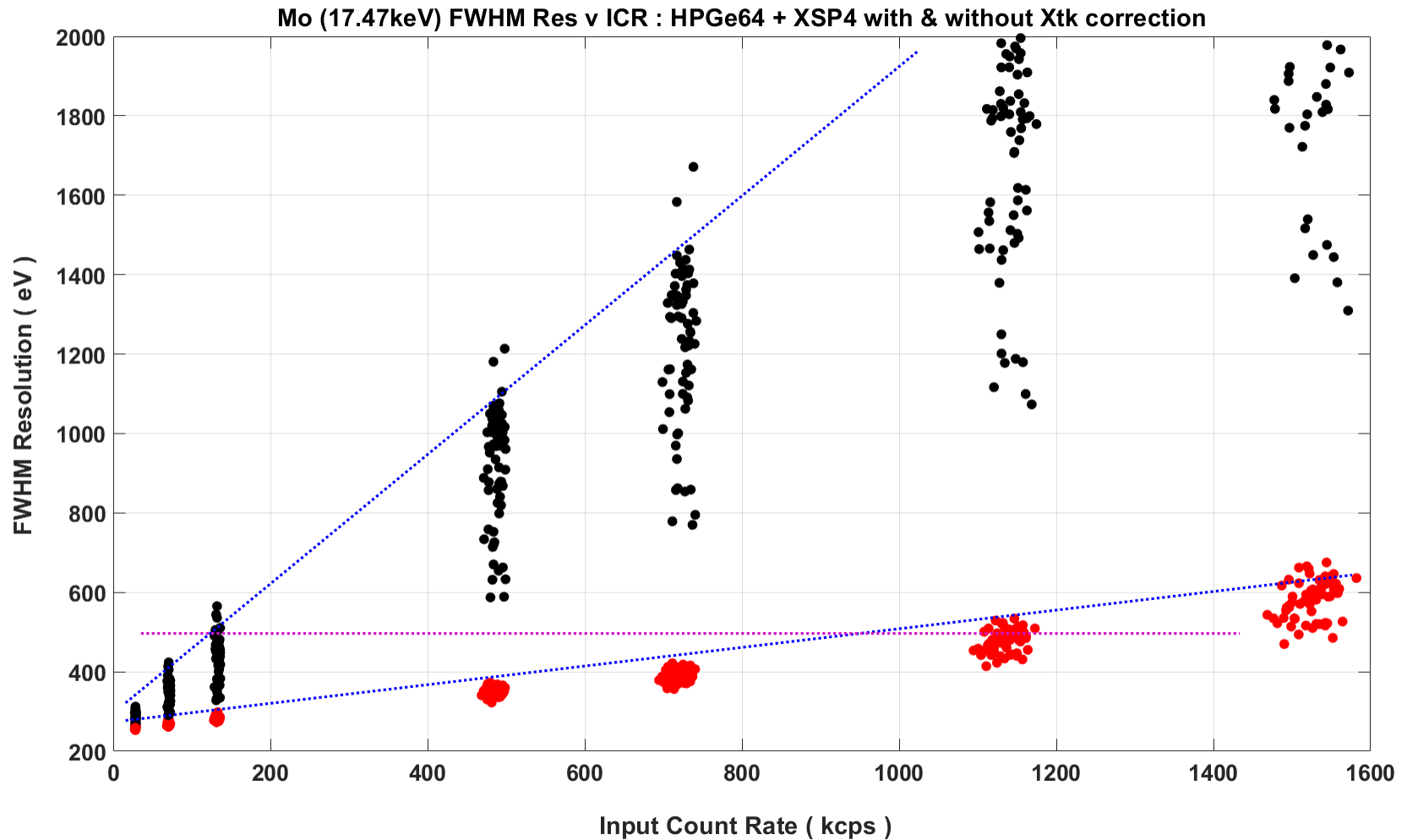
MCA Mo (17.47keV) @ 776kcps OCR HPGe64 + XSP4 : Chan 10



All 64 pixels – Mo Resolution against Output Count Rate



All 64 pixels – Mo Resolution against inferred **Input Count Rate**

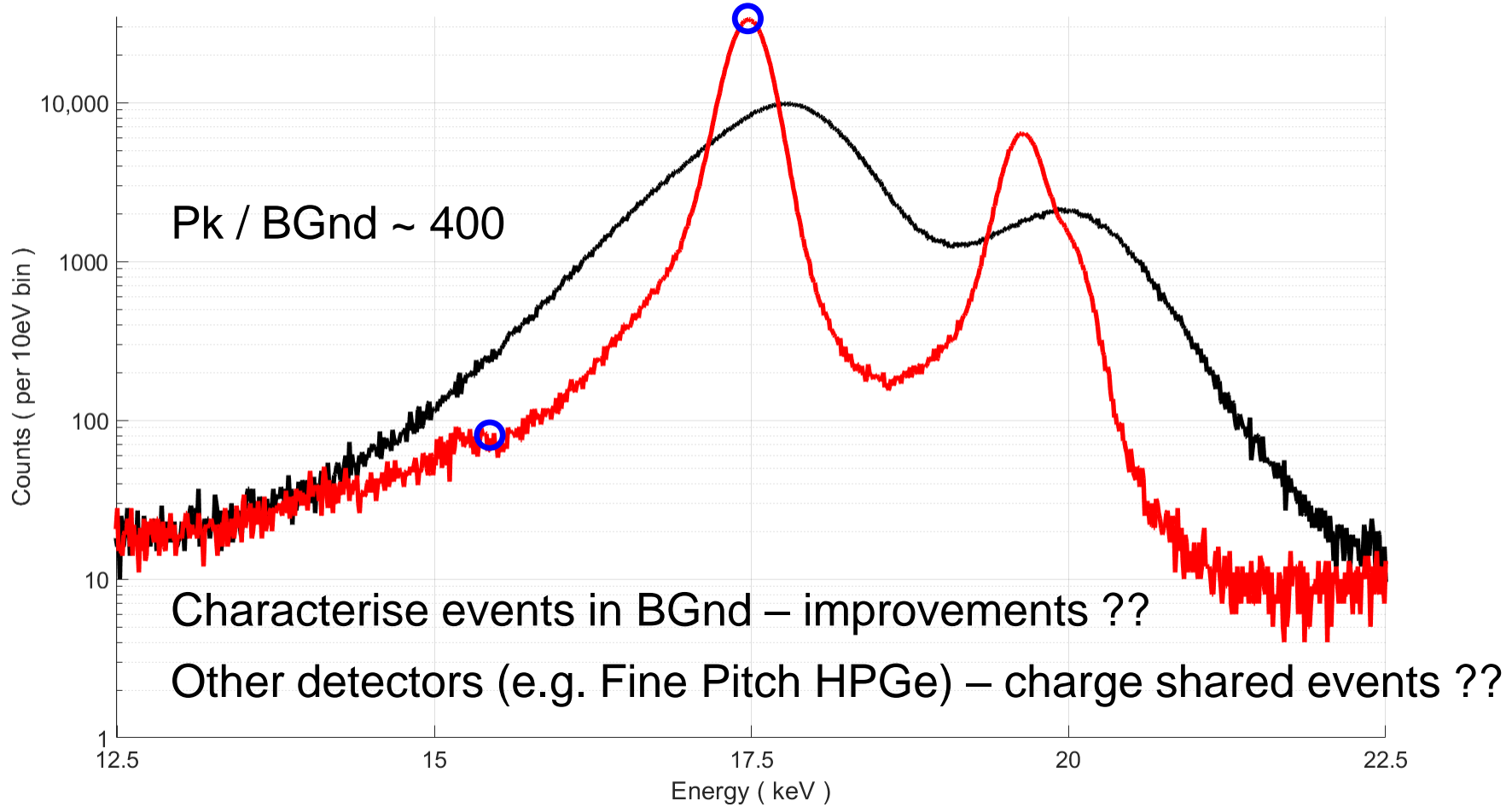


ICR 170kcps → 950kcps @ FWHM < 500eV...is good, but...



Back to Mo 400kcps: Pk / BGnd improvement & thoughts for the future...

MCA Mo (17.47keV) @ 414kcps OCR HPGe64 + XSP4 : Chan 10



Concluding Remarks...

With knowledge of the local neighbourhood at *both calibration and run time* very useful performance gains are possible...

- Event XTK Correction 😊

Chan-to-Chan Communication across many channels (not just those sharing a single FPGA!!) will be useful to study other neglected areas of detector performance...

- Background (Low Energy Tail) Reduction ?
- Charge Sharing Identification and “correction” ?
- Other features (...as yet undiscovered) ?

Xspress 4 Project Team - Acknowledgements

DLS Detector Group

Sudeep Chatterji (Detector Scientist)
Graham Dennis (Electronics Engineer & PM)
Ian Horswell (Electronics Engineer)
David Omar (Electronics Engineer)
Jonathan Spiers (Technician)
Nicola Tartoni (Group Leader)

STFC

Darren Ballard [RAL] (PCB Layout)
William Helsby [DL] (Firmware Engineer)
Adam Davis [RAL] (FEM2 design)

Other DLS Groups

Nic Bricknell (SW Systems Engineer - EPICS)
Iain Hall (Data Acquisition Scientist - GDA)
Steve Alexander (Project Planner)
Sofia Diaz-Moreno (I20 Principle Scientist & Customer)
Shu Hayama (I20 Scientist)

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