# Power-aware design

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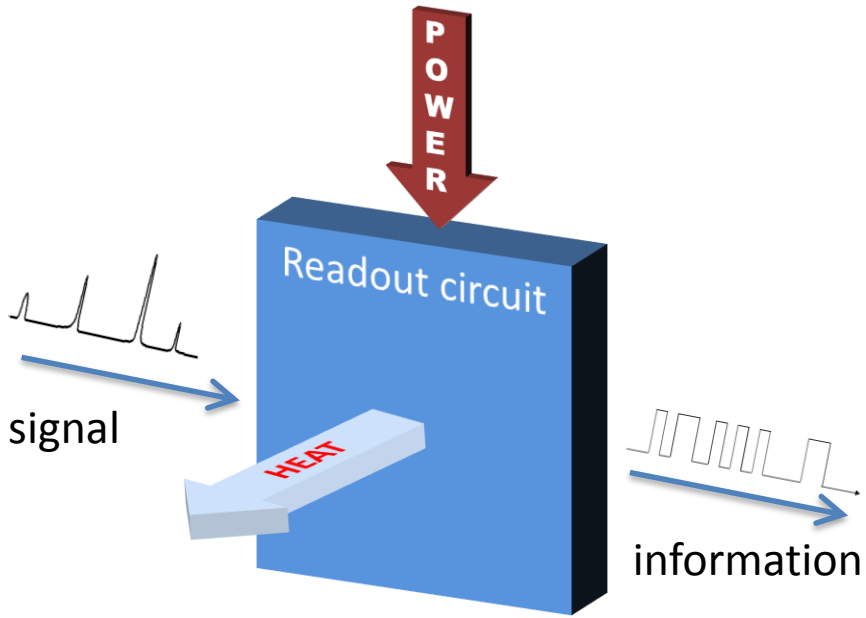
IFDEPS 2018 Annecy

# Importance of power planning

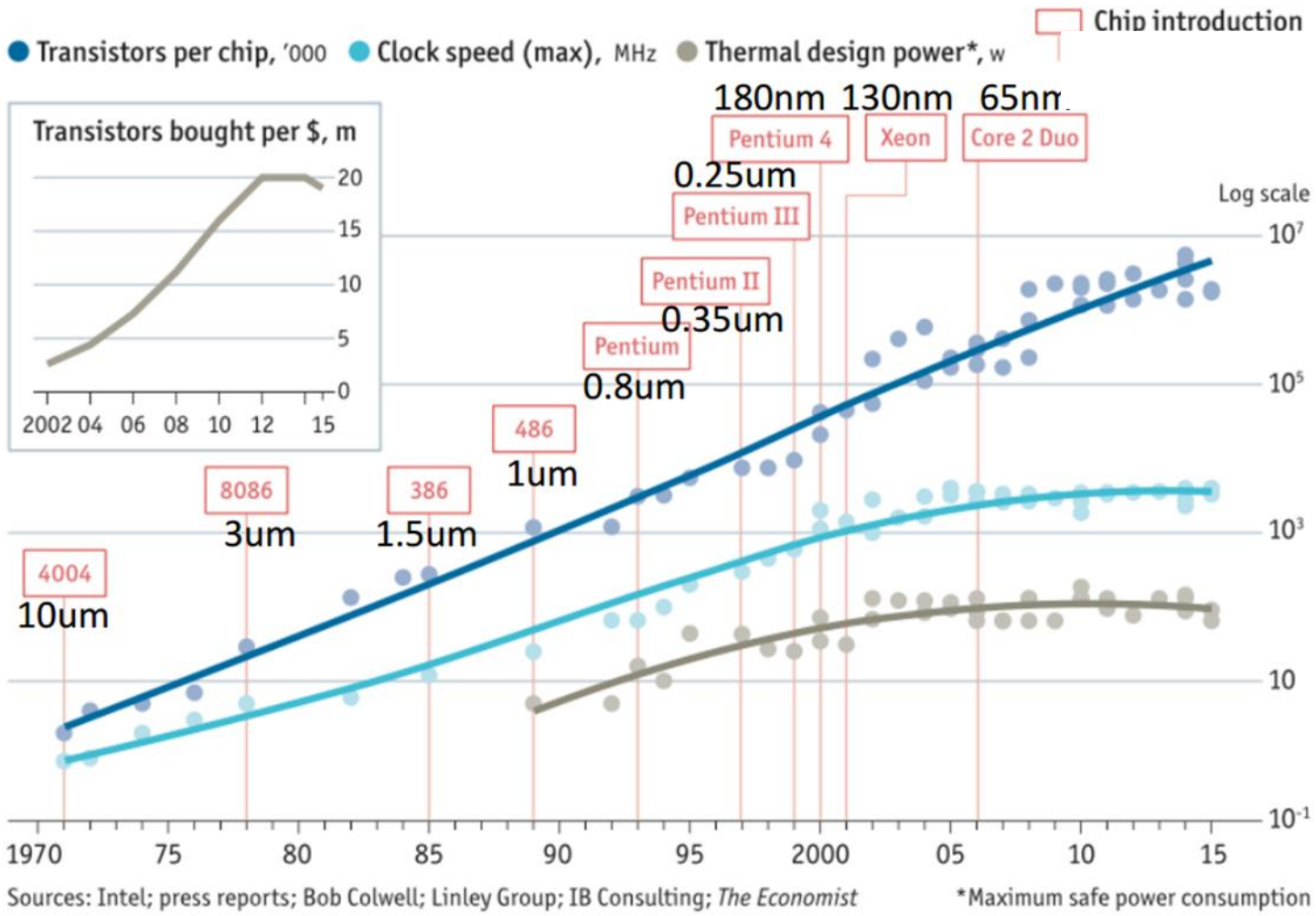
- Electronic circuits are usually regarded as manipulators of signals and information
- Frequently neglected is that they are also thermodynamic machines and the electrical manipulations incur a cost in power dissipation

Awareness of power tradeoffs is needed at the transistor/technology, circuit, and system level:

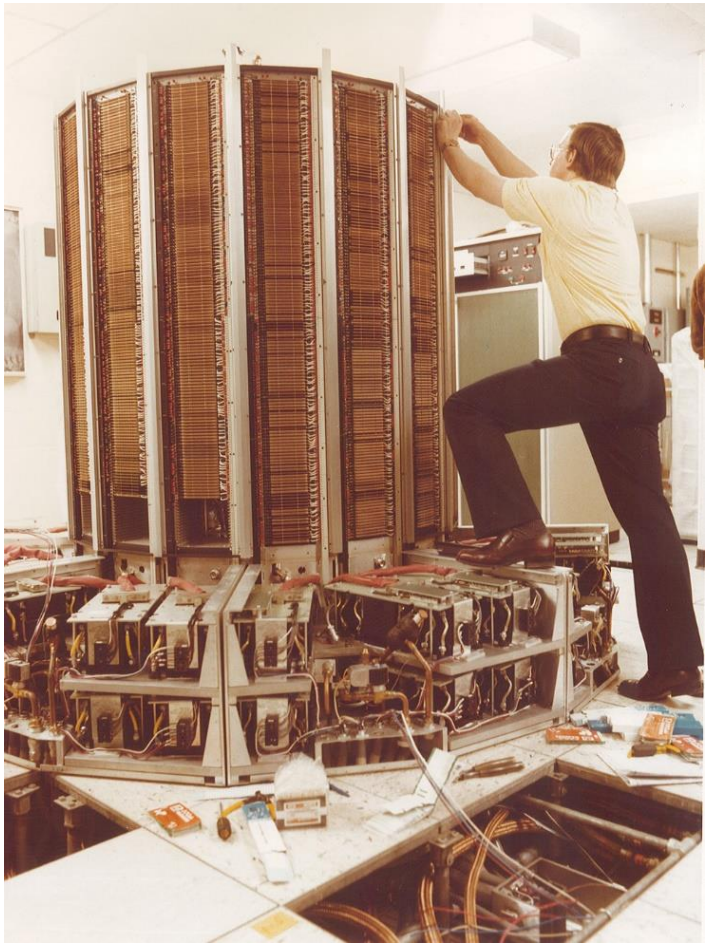
- ***Many performance parameters have a steep dependence on expended power***
- ***For large, highly integrated systems it is easy to underestimate the engineering challenges of managing power delivery and heat removal***



# Microprocessor speed and power trend



# Cray-2 supercomputer (1985)



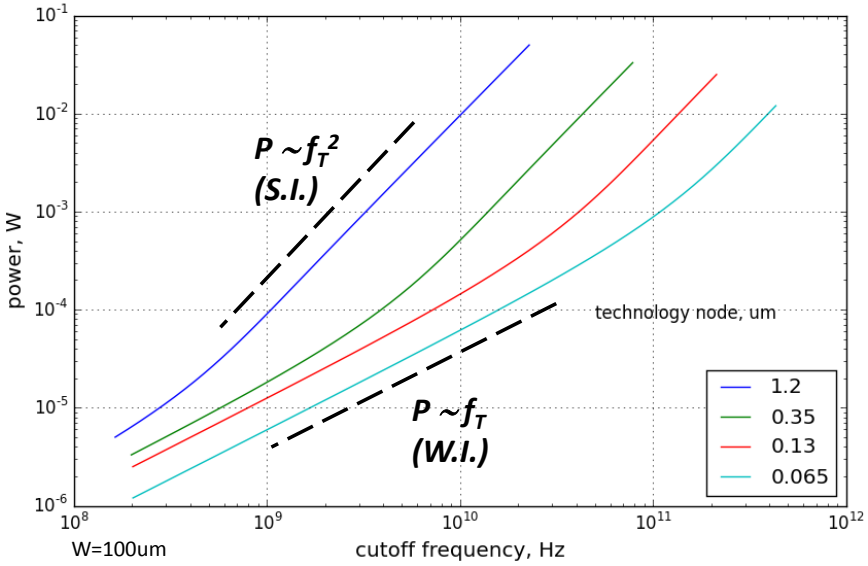
- 4 processors
- 1.9 GFLOPS peak
- Clock speed 0.25GHz
- 2500kg
- 200kW

Logic module

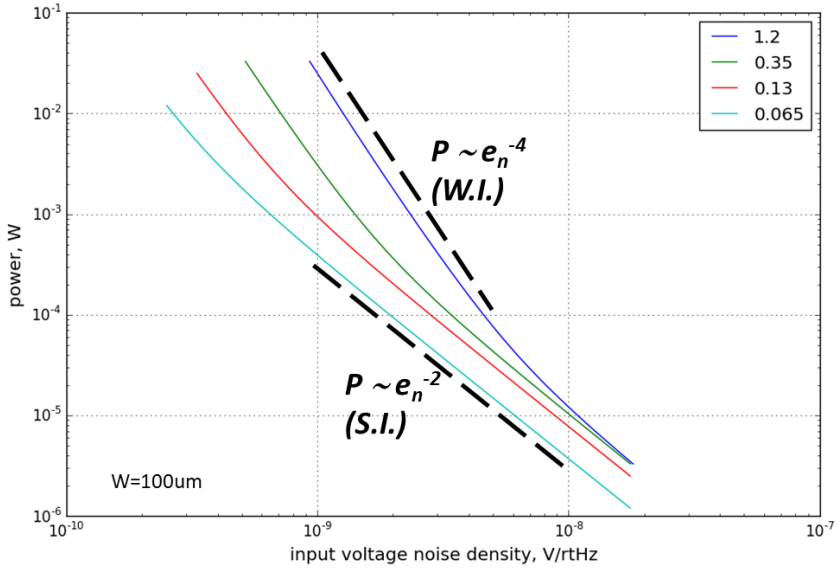
# Transistor power vs. speed and noise

- In analog CMOS, designer selects technology feature size, transistor geometry (gate length and width), transistor polarity (NMOS/PMOS), and bias current
- Current density (I/W) determines state of inversion (weak/moderate/strong)
- In deep submicron technologies, weak/moderate inversion is typical bias condition

Power vs. cutoff frequency

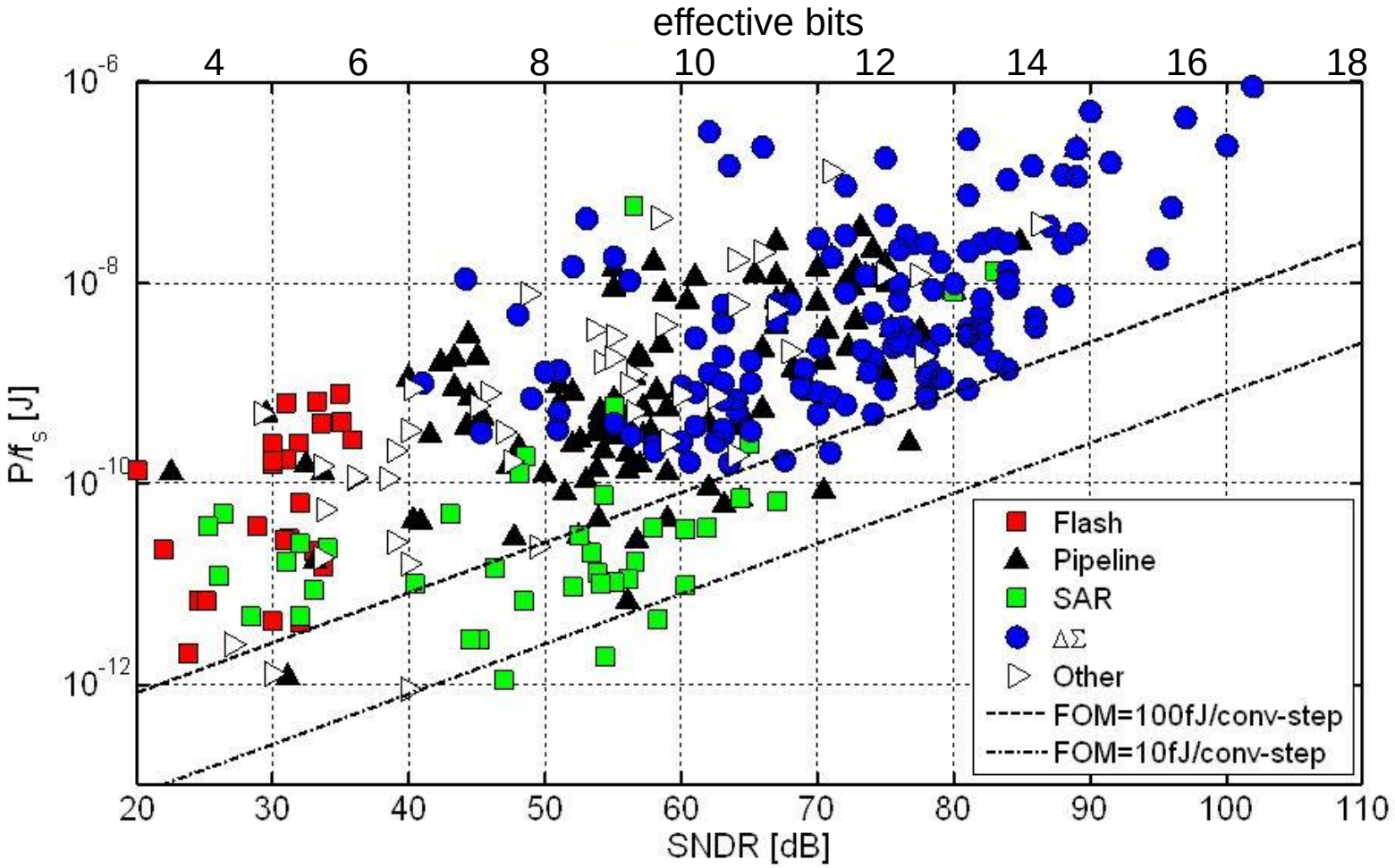



Power vs. input noise density



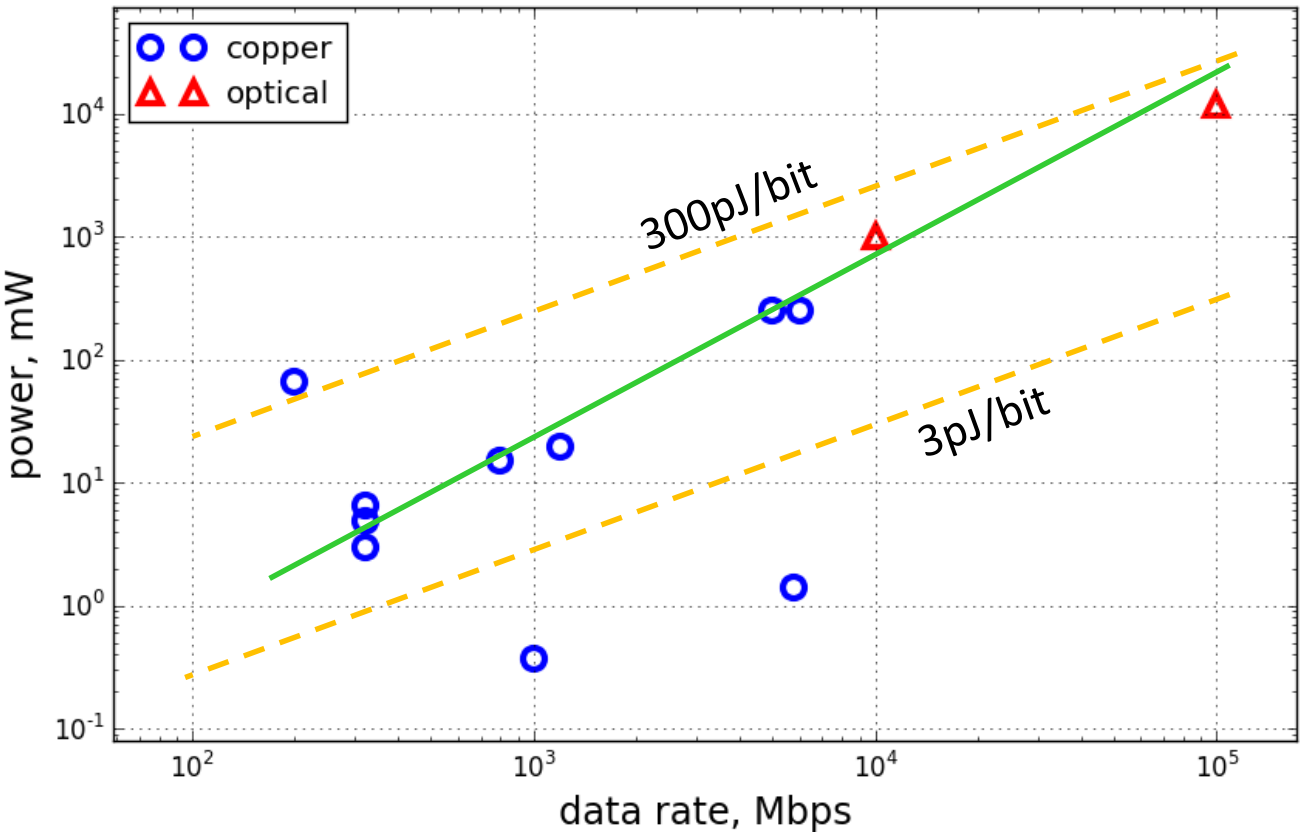
# Analog-to-digital conversion energy

- Figure-of-merit for AD converters (energy per conversion): $\boldsymbol{FOM = \frac{P_{diss}}{f_s}}$
- Thermal limit: $\boldsymbol{\frac{P}{f_s} \geq 4 \cdot kT \cdot SNR}$




Murmann 2008

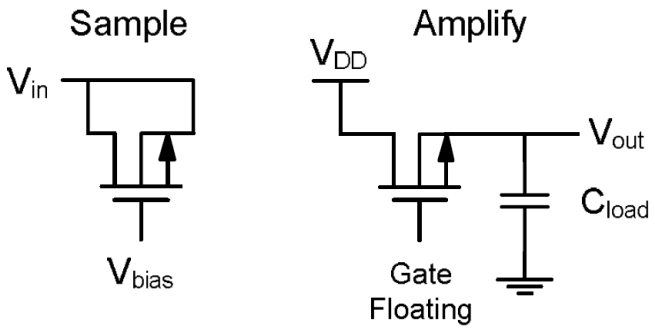
# Digital data link power



# Digitally-assisted analog

- in 90nm CMOS, more than 2,000,000 gates would need to switch to consume the energy an A/D conversion at 16b resolution
- It pays to take advantage of the availability of abundant digital resources to enhance the performance and precision of analog circuits
  - Mismatch correction
  - Nonlinearity correction
  - Correction of dynamic errors allowing the use of "mimimalistic" analog topologies

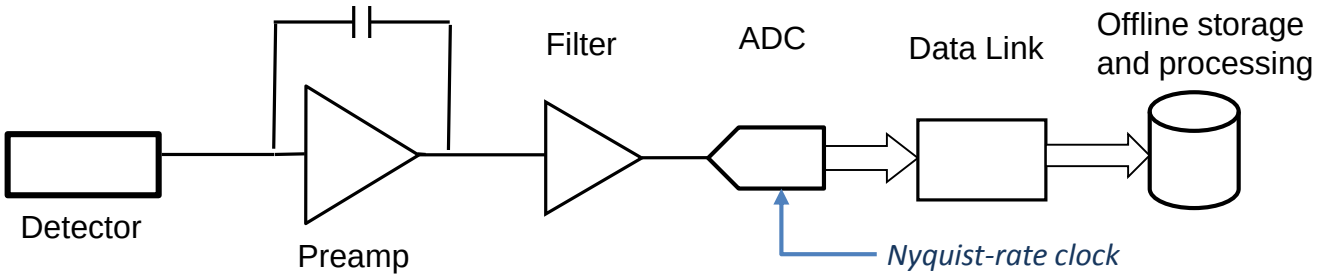
Single-transistor residue amplifier




*B. Murmann, "A/D Converter Trends: Power dissipation, scaling and digitally assisted architectures", IEEE 2008 CICC 7-5-1*
*J. Hu et al., "a 9.4bit, 50MS/s, 1.44mW pipelined ADC using dynamic residue amplification", Dig. VLSI Circuits Symposium, Jun. 2008*

# Is there more efficient way to extract the information in the signal?

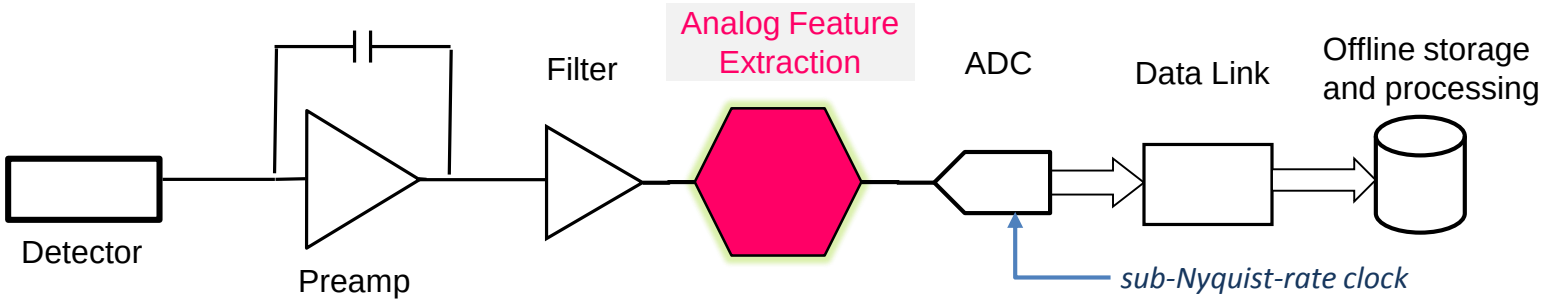
## Conventional signal chain




Raw: 15MB

JPEG: 150KB

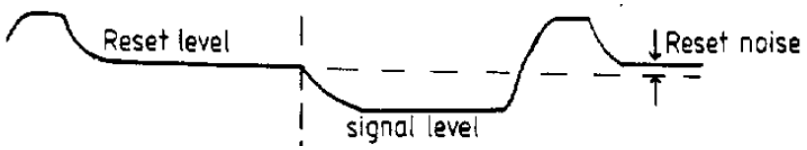
*One can regard the possibility of digital compression as a failure of sensor design.*
*If it is possible to compress measured data, one might argue that* ***too many measurements were taken***
*-- David Brady*



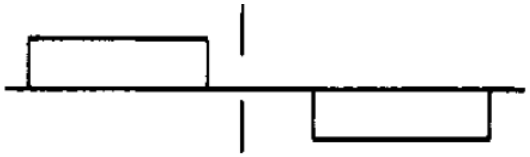
# Measurement of step height (CCD)

*Dual-slope integrator (differential averager) is the matched filter for step waveform with white noise*
*As long as the pixel frequency is greater than the 1/f noise corner, noise is within 5% of ideal*

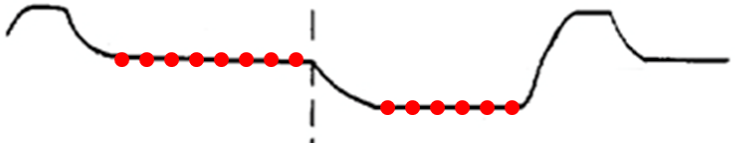
## CCD signal




## Optimal filter



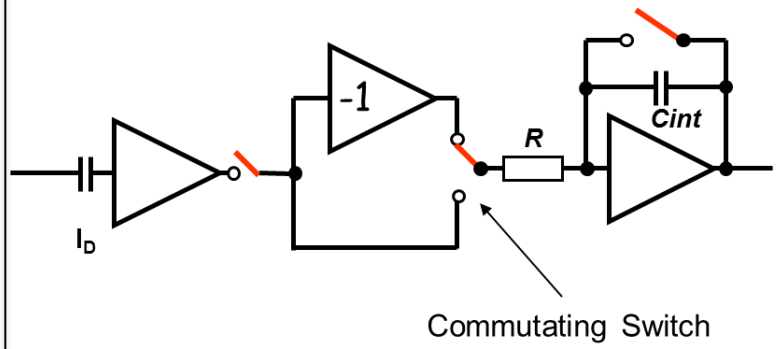
## Digital CDS implementation



*~20 samples/pixel*

Total energy per pixel:
20 × 10.7nJ + 360b × 100pJ/bit = ***250nJ***

## Analog dual-slope integrator

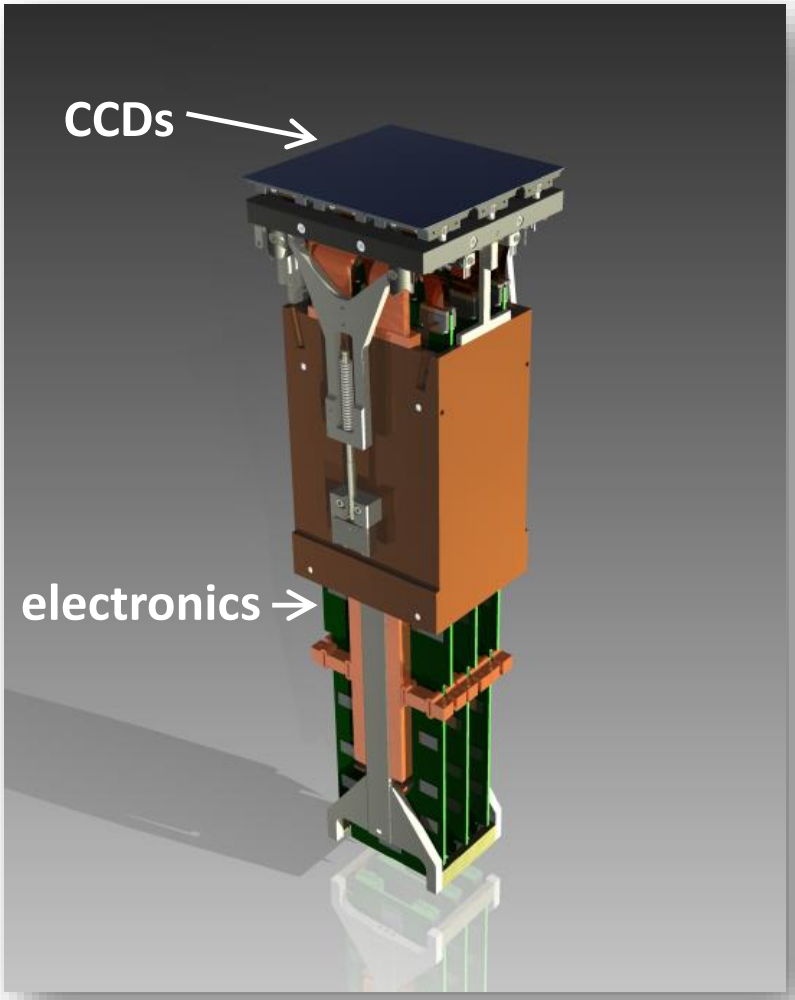




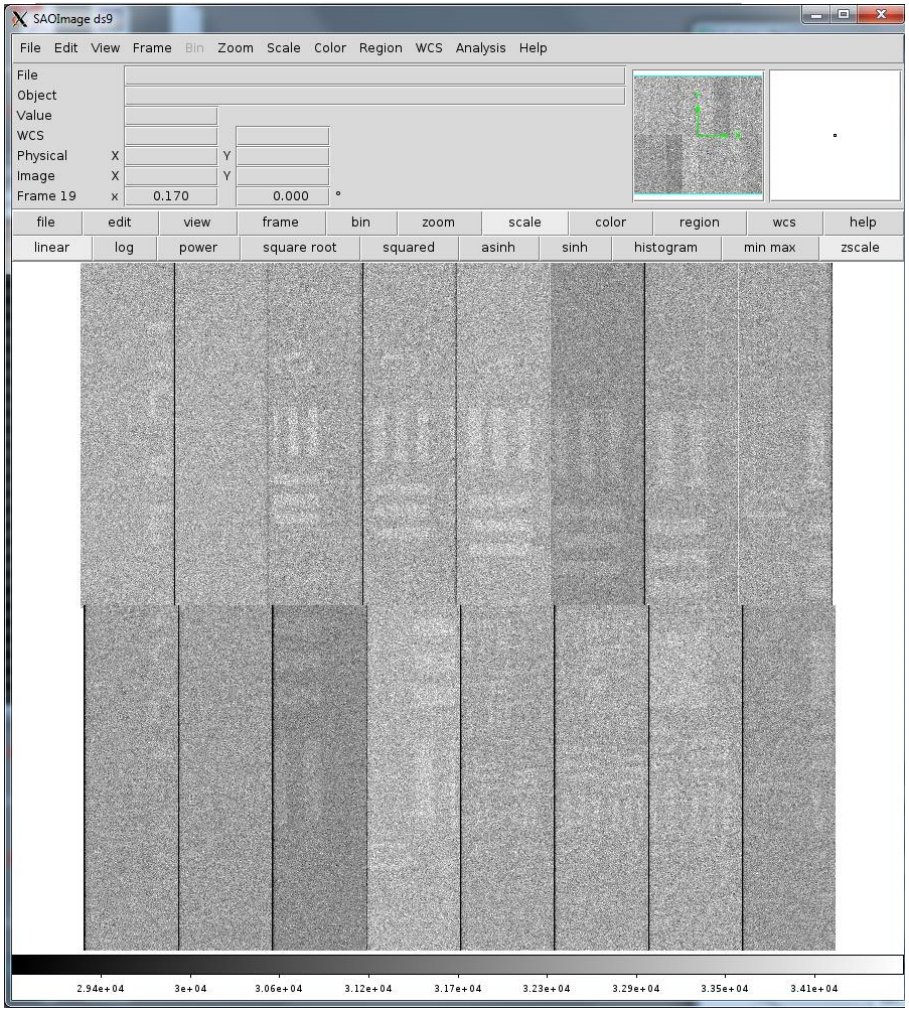
*1 sample/pixel*

Total energy per pixel:
35mW/560kHz + 1 × 10.7nJ + 18b × 100pJ/bit = ***75nJ***

# LSST Raft Tower Module

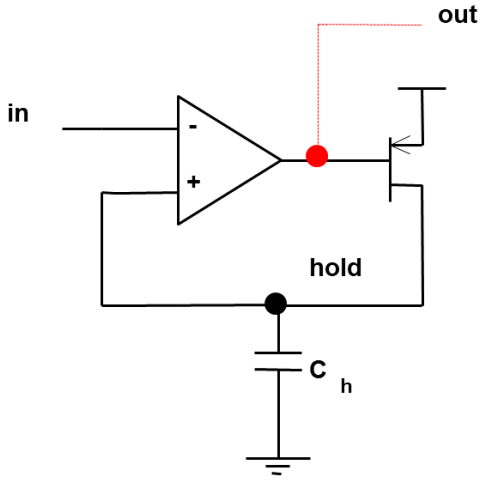


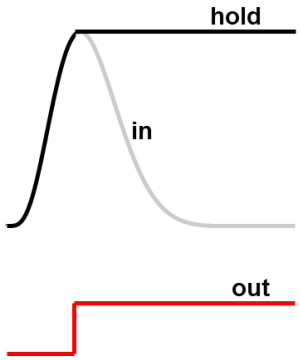

***Photons in – bits out***




Signal = 4e- mean
Noise = 7e- rms

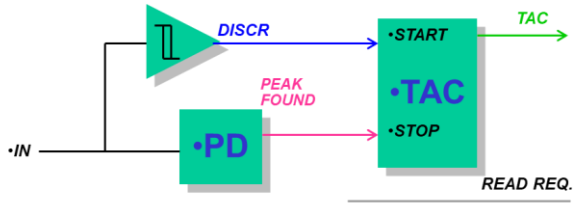
# CMOS peak detector

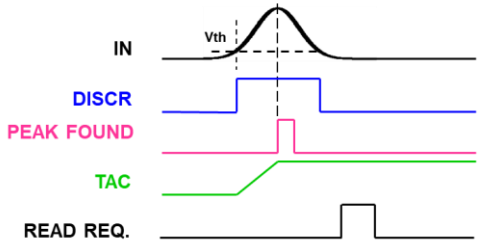


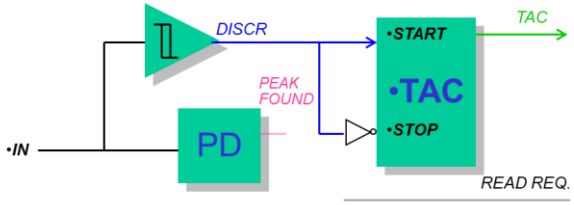

$V_{out}$ is free of time-walk

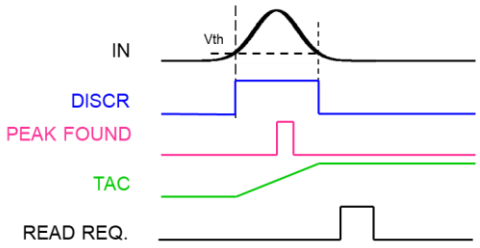
## Risetime



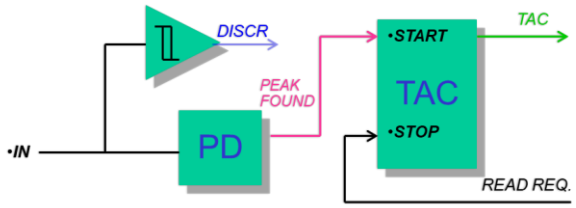



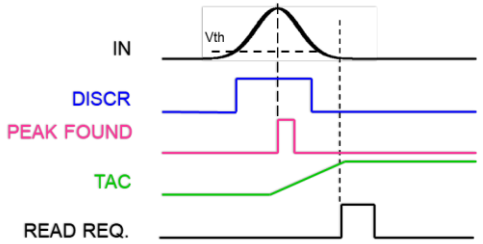

## Time-over-threshold



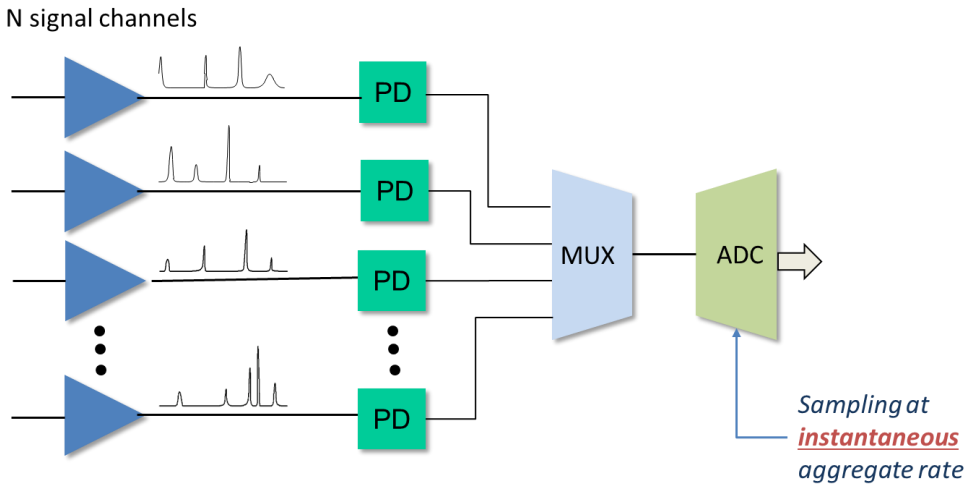

## Time of occurrence



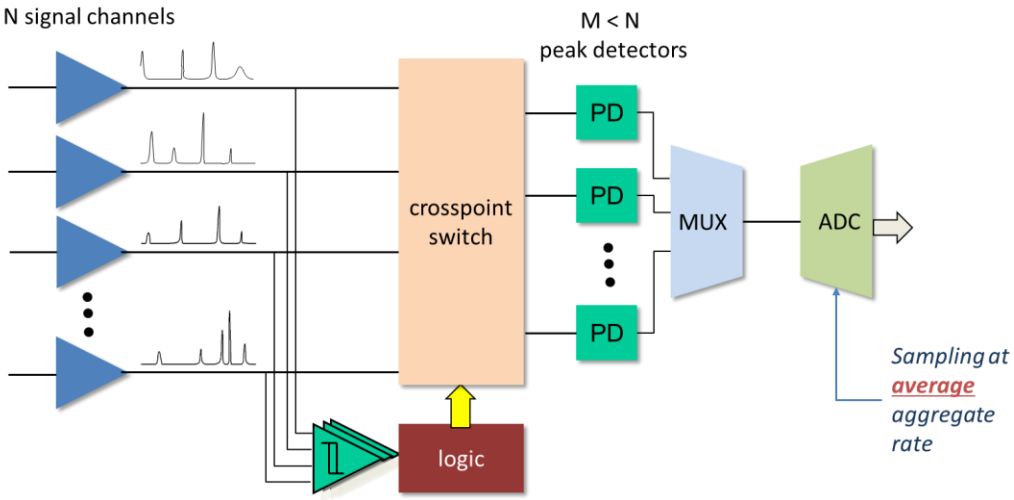



# Multichannel system – sharing of peak detectors

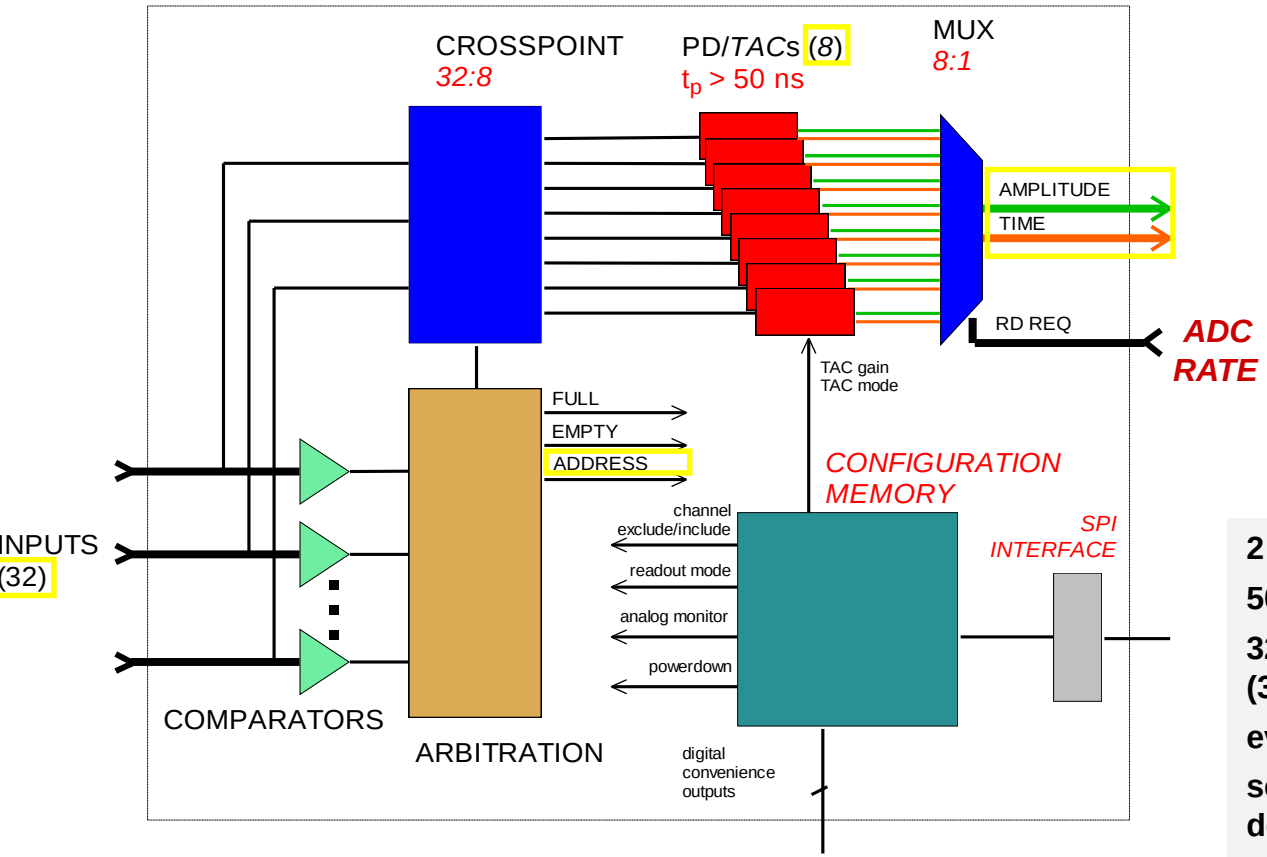
## Peak detector per channel




## Shared peak detector bank with activity detection



# SCEPTER ASIC




**2 mW / channel**

**50 MS/s rate capability**

**32:1 multiplexing of shaped input signals (30ns peak time)**

**event amplitude, timing, address**

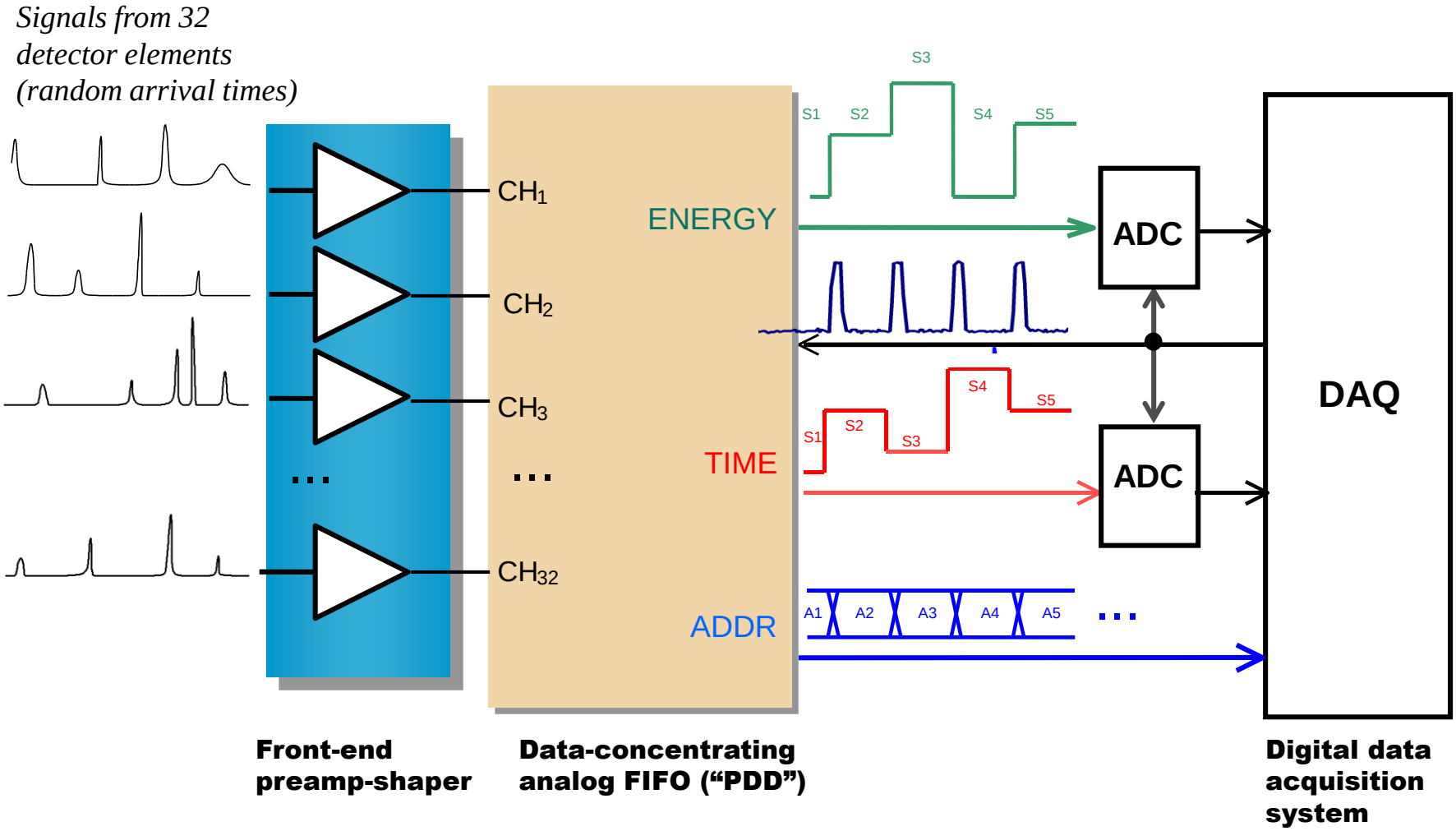
**self-triggering, sparsification, derandomization, data concentration**

**0.35um CMOS 3.3V**

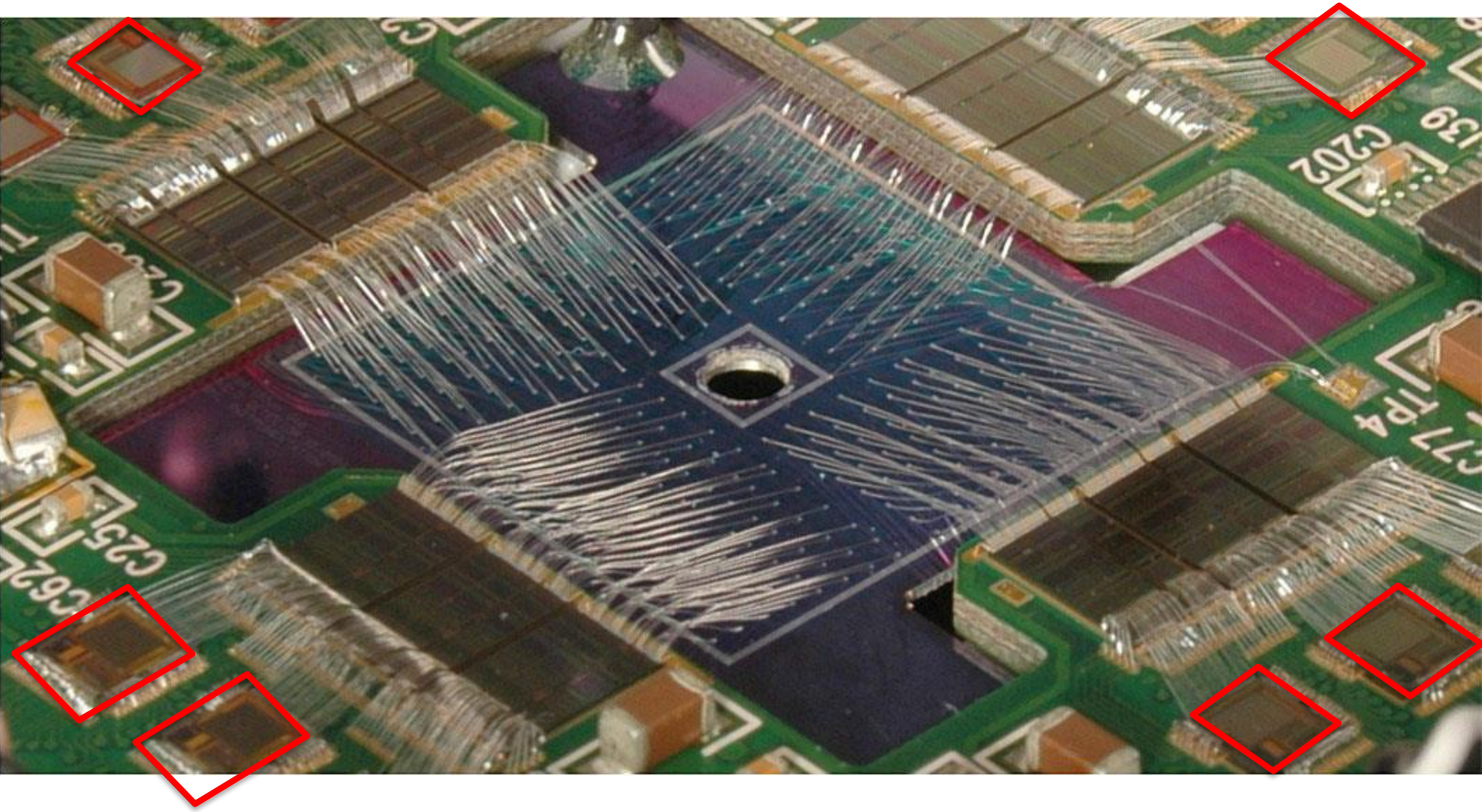
**3.2 x 3.2 mm$^2$**

P. O'Connor, G. De Geronimo, A. Kandasamy, IEEE Trans. Nucl. Sci. 50(4), pp. 892-897 (Aug. 2003).

# Peak- and time-detector with analog derandomization



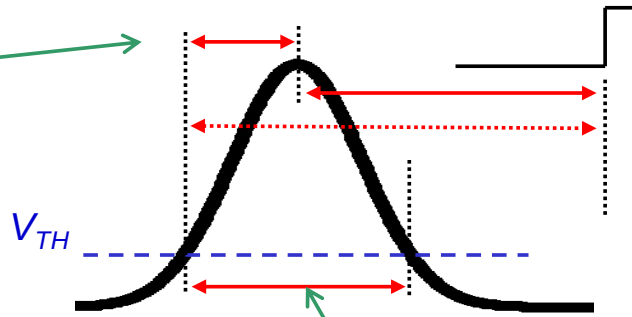
# SCEPTER ASIC in MAIA Detector



# SCEPTER measurements

Peaking Time

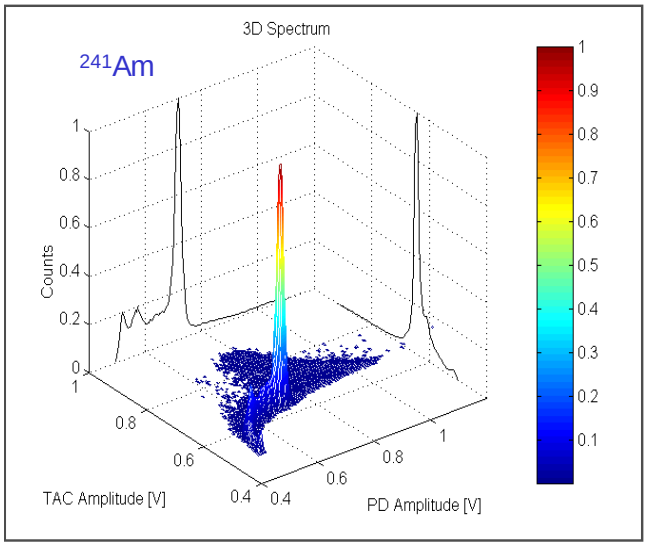
Sensor:
CZT pixelated linear array
32 elements, 16x3x3 $mm^3$
Rate:
~ 4.5 Mcps overall
~ 210 kcps single pixel
Resolution:
~ 3.4% (2.0keV) @ 60 keV



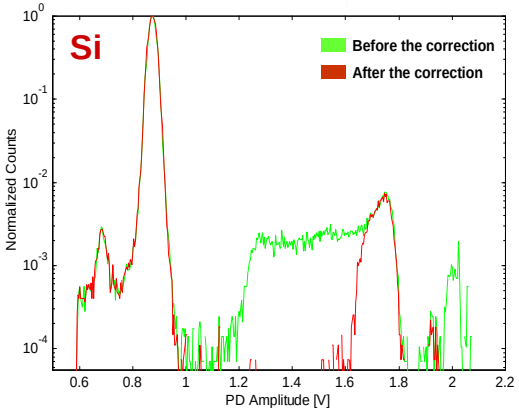

Read Request

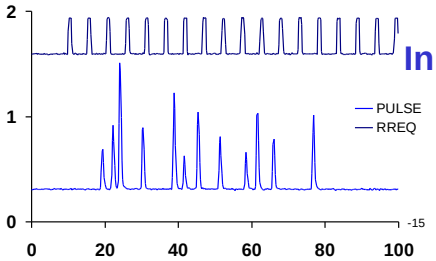
Time **of Occurrence**

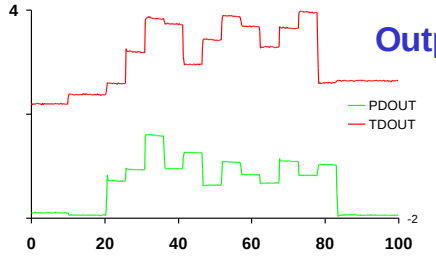
Time-Over Threshold

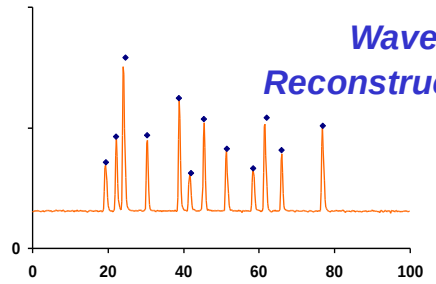



***Pile-Up Rejection***




Dragone, A., De Geronimo, G., Fried, J., Kandasamy, A., O'Connor, P., Siddons, D. P., Corsi, F. (2006). Pile up rejection and multiple simultaneous events acquisition with the PDD ASIC. In Research in Microelectronics and Electronics 2006, Ph. D. (pp. 381-384). IEEE.

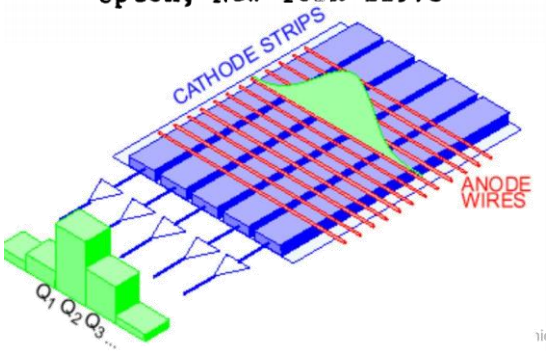
# Analog centroid-finding filter

- Computes centroid of charge from split event
  - Applied to gas proportional chambers with charge-sharing across strips or wires
  - Generally applicable to any interpolating position-sensing readout
- Minimizes noise by using only those outputs containing centroid information
- Analog convolution of sequentially-switched samples with “N” filter: zero-crossing time proportional to first moment of the charge distribution
- Position accuracy and linearity significantly improved over resistive or RC charge division methods.

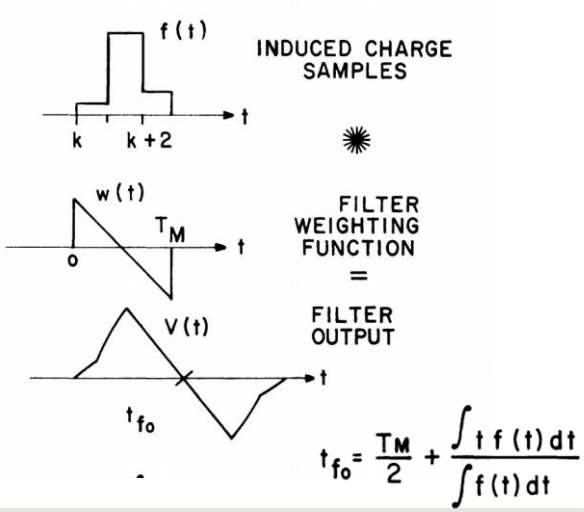
CENTROID FINDING METHOD FOR POSITION-SENSITIVE DETECTORS*

V. Radeka and R. A. Boie

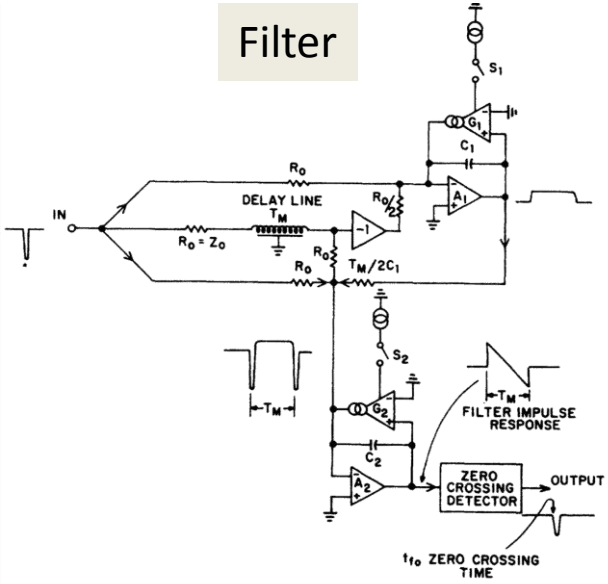
Brookhaven National Laboratory
Upton, New York 11973



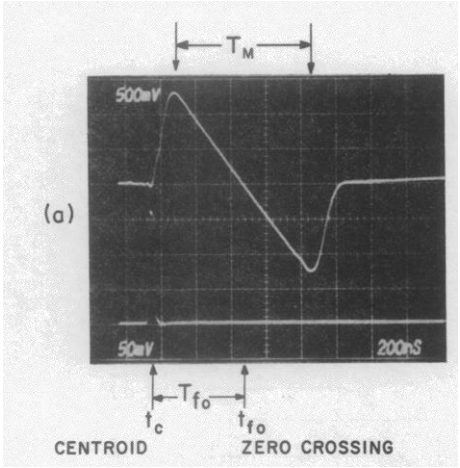

## Principle




## Filter

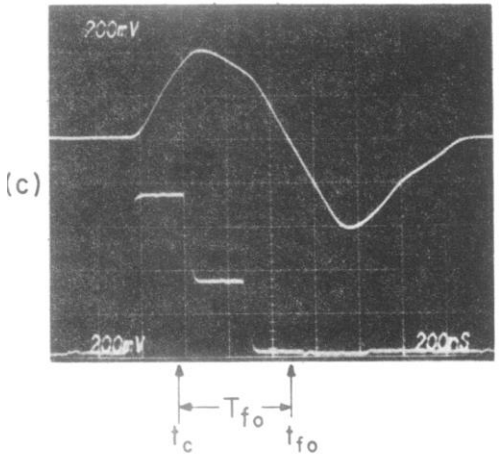



## Impulse response

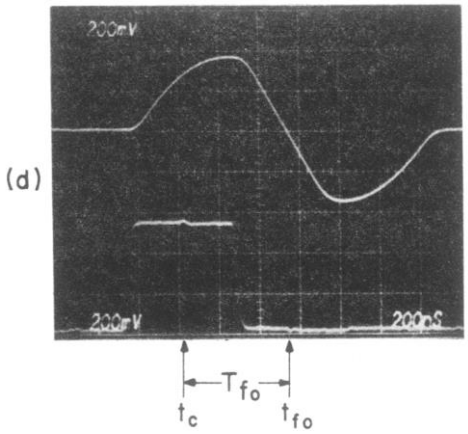


# Analog centroid finder performance

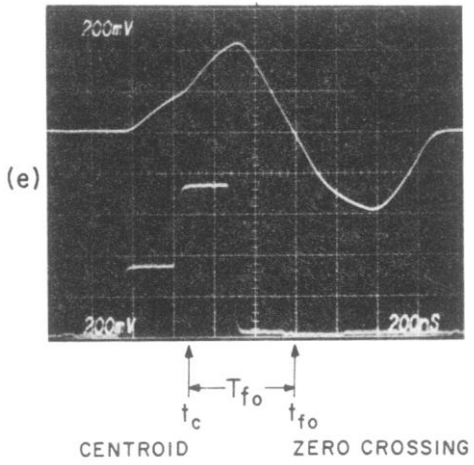
x/L = 0.3



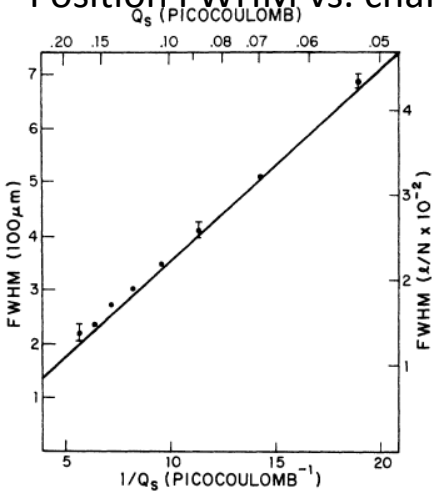

x/L = 0.5



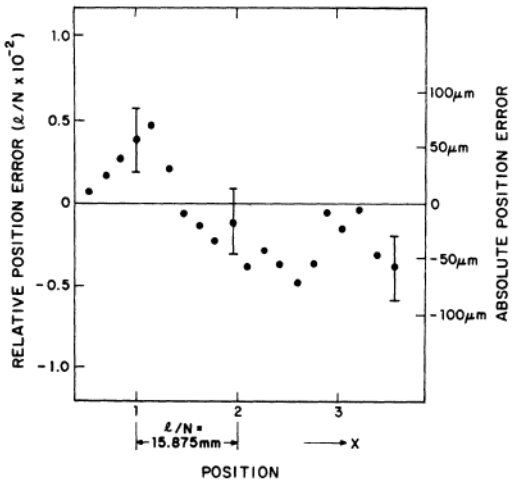

x/L = 0.7



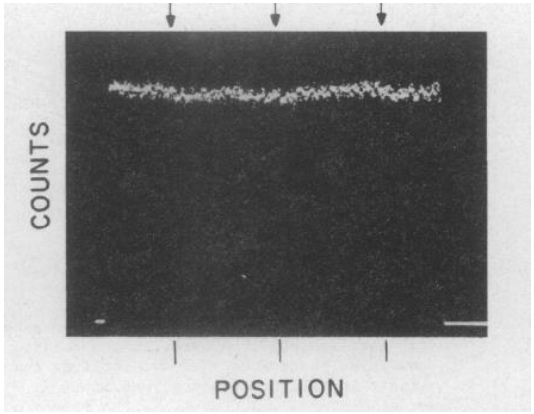

Position FWHM vs. charge




Integral nonlinearity




Differential nonlinearity



# Power-aware design: key ideas

- Understand power-efficient transistor sizing/biasing in chosen technology
- Capture information content of signal with minimum-rate, minimum-resolution sampling
- Extract features in analog domain upstream of ADC
- Use analog buffering for derandomization
- Use activity detection and pooled resources
- Follow development of commercial sensor interfaces requiring low power and low latency: mobile, wearable, implantable, always-on, radar, voice processing, …


THANK YOU!

# References


- Murmann, B. “A/D Converter trends: power dissipation, scaling, and digitally-assisted architectures”, Proc. IEEE Custom Integrated Circuits Conf. 2008
- O’Connor, P., DeGeronimo, G., “Prospects for charge sensitive amplifiers in scaled CMOS”, Nucl. Instrum. Meth. A480 (2002), 713-725
- Radeka, V., Boie, R.A., “Centroid Finding Method for Position-sensitive Detectors”, IEEE Trans. Nucl. Sci. 27 (1980), 351-362
- Antilogus, P., et al. "LSST camera readout chip ASPIC: test tools." *Journal of Instrumentation* 7.02 (2012): C02044.Antilogus, P., et al. "ASPIC: LSST camera readout chip. Comparison between DSI and C&S." *Topical Workshop on Electronics for Particle Physics (TWEPP-09)*. 2009.
- De Geronimo, Gianluigi, Anand Kandasamy, and Paul O'Connor. "Analog peak detector and derandomizer for high-rate spectroscopy." *IEEE Transactions on nuclear science* 49.4 (2002): 1769-1773.
- O'Connor, Paul, Gianluigi De Geronimo, and Anand Kandasamy. "Amplitude and time measurement ASIC with analog derandomization: first results." *IEEE Transactions on Nuclear Science* 50.4 (2003): 892-897.
- Dragone, A., De Geronimo, G., Fried, J., Kandasamy, A., O'Connor, P., Siddons, D. P., ... & Corsi, F. (2006). Pile up rejection and multiple simultaneous events acquisition with the PDD ASIC. In *Research in Microelectronics and Electronics 2006, Ph. D.* (pp. 381-384). IEEE.