





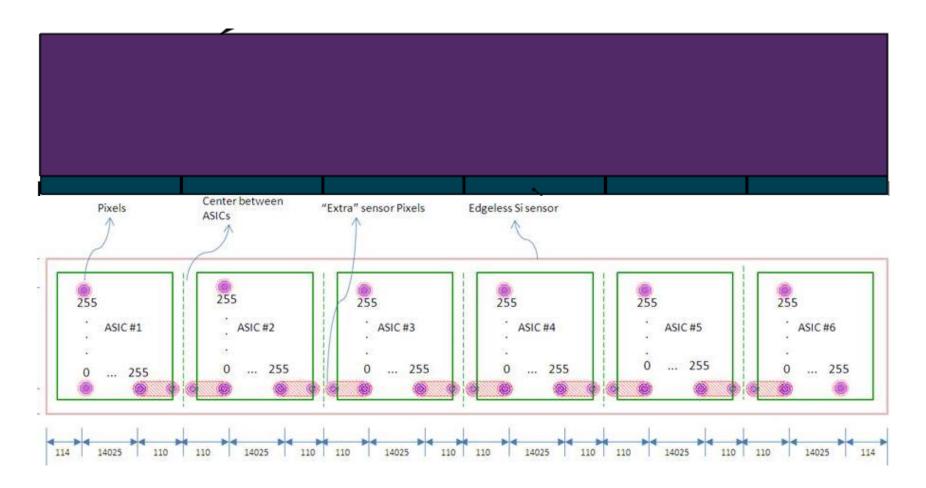


Medipix detectors developments at the Brazilian Synchrotron Light Laboratory LNLS for Sirius

CNPEM – LNLS Detectors Group (jean.polli@lnls.br), March, 12th 2018





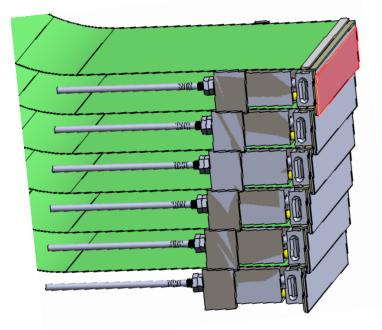


- 6x1 Medipix3 ASICS monobloc Si Edgeless sensors thickness with 300um or 675um
- 0.4 Megapixels
- No gaps between ASICS columns Projected to comport bigger areas



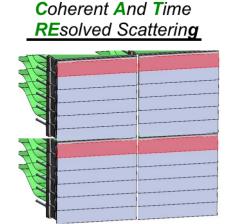


PIMEGA project - Head Stackable Module



- 2.4 megapixel x-ray detector module based on 6 x HEXA sensors. Total of 36 Medipix3 ASICS

- A stack of HEXA modules in a stairs shape
- This assembly covers the wirebonding and protects ASICS periphery against high radiation dose.
- No detection gaps neither Rows nor columns
- 85x85mm 100% active area
- Low vacuum compatible 10-3 mbar
- Simple exchange modules for maintenance



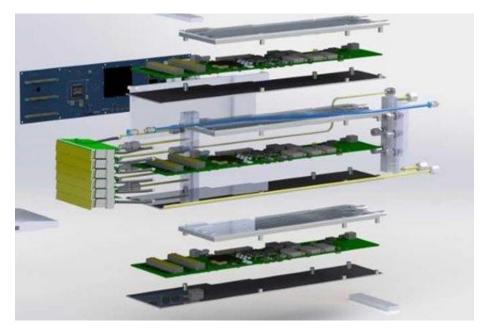
CATERETÊ

- Projected to comport bigger areas with submilimeter gaps between modules
- 9.4 megapixel detector based on 4 PIMEGA modules for Caterete and Manacá beamlines

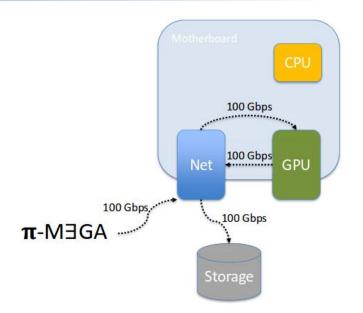




PIMEGA project - Front-end + Back-end



- Up to 2000 fps at 12 bit in continuous read/write mode
- Low vacuum compatible front-end and control electronics
- Data transfer through 100 m optical fiber 100 Gbps band data throughput
- Projected to comport either bigger or smaller areas using same hardware



- Data transfer through 100 m optical fiber Network Link with 100 Gbps band data throughput (ROCE implementation)
- IBM HPC (OpenPOWER 8, 9)
- This server backend interface directly linked to the memory and GPUs (graphical processing units)



СИРЕШ







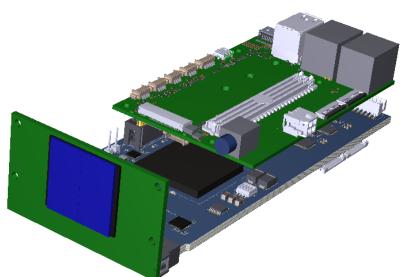
- 800 Kpixels (2 rows x 6 columns) X-ray detector based on Medipix3RX ASIC with Si sensors
- Up to 600 fps at 12 bit in continuous read/write mode
- Low vacuum compatible front-end and control
- Electronics (uses same readout board of PIMEGA module)
- Data transfer through 10 Gbps Ethernet fiber optics data throughput with server backend interface

Mobipix Detector

- 260 Kpixels x-ray detector
- 2x2 Medipix3 ASIC with Si or CdTe sensors.
- Up to 2000 fps at 12 bit in continuous read/write mode
- Low vacuum compatible front-end and control electronics (uses same FPGA and low level control software of the PIMEGA Module)
- Self conteined, Data collection and processing inner detector with GPUs cores

SCIENCE, TECHNOLOGY

INNOVATION AND COMMUNICA





Acknowledgments



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