European Synchrotron Radiation Facility

Computing Services - Electronics Group

CS/EL/05-02

ASG217 data sheet (preliminary)

last update 01/12/06 by C. Hervé

ASG217 main parameters

ASG217 is a 16 channel pre-amplifier/discriminator to meet the requirements for parallel binary readout of gaseous detector like wire chambers. Each individual channel features a DAC for fine discriminator threshold setting. Discriminator output are PseudoLVDS (LVDS like @ 2 mA driving current). All ASG217 parameters are thereafter reported for a 50 uA IREF current, a 3.3 Volts analog supply voltage and a 2.5 Volt digital supply voltage. The preamplifier may be tuned in gain (high or low) and bandwidth (high or low).

ASG217 preamplifier tuning dependent parameters

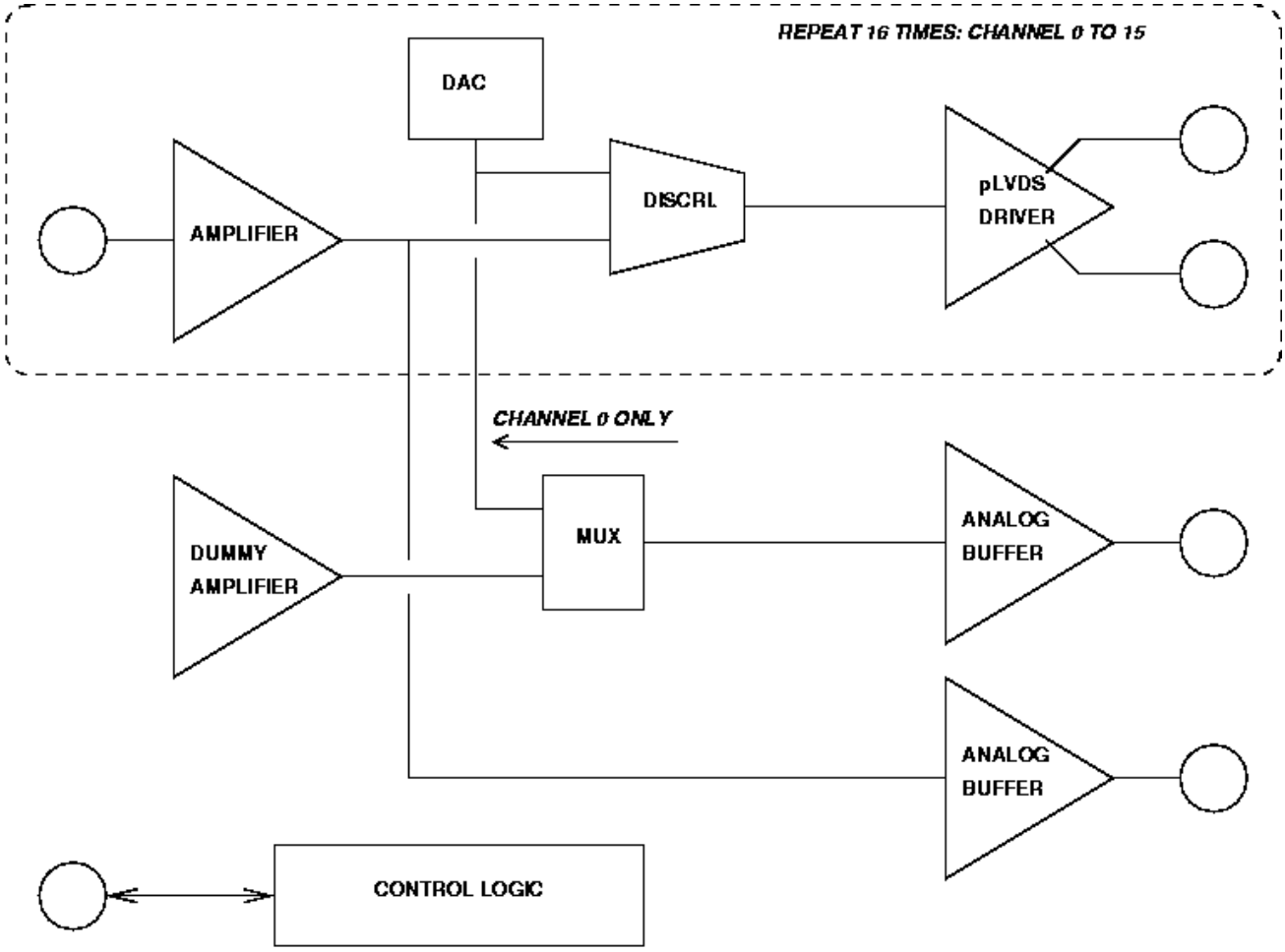
Parameter	High gain, high BW	High gain, Low BW	Low Gain, High BW
Pre-amplifier: trans-impedance gain (equivalent charge amplification is given @20ns peaking time)	220 KOhms 11 mV/fC 1.8 uV/e	220 KOhms 11 mV/fC 1.8 uV/e	130 KOhms 6.5 mV/fC 1.05 uV/e
Pre-amplifier: bandwidth (@3dB, @ zero capacitance input)	16 MHz	10 MHz	18 MHz
Pre-amplifier: peaking time (@90%, @ zero capacitance input)	11 ns	13 ns	10 ns
Pre-amplifier: output noise RMS (@ Iref = 50uA)	1.5 mV + 0.1 mV/pF	1 mV + 0.07 mV/pF	1 mV + 0.07 mV/pF
Pre-amplifier: ENC (RMS @20 ns peaking time, @ Iref = 50uA)	470e + 32 e/pF	320 e + 23 e/pF	320 e + 23 e/pF
Pre-amplifier offset between channels	± 60 mV max.	± 60 mV max.	± 40 mV max.
Crosstalk from all odd outputs fired to channel zero input feedback	± 6 mV max.	± 6 mV max.	± 4 mV max.

ASG217 other main parameters

Next table reports on the common parameters, largely independent from the preamplifier tuning.

Number of channels	16
Pre-amplifier: input resistance	75 Ohms
Discriminator: threshold adjustment range	150 mV or 280 mV selectable, typical value
Discriminator hysteresis	12 mV or 30 mV selectable, typical value
Input event rate	20 MHz per channel max.
Technology	0.35 um SiGe
Package	TQFP100, 0.5 mm pitch
Pre-amplifier supply	3.3 V to 4.0 V
Discriminator and logic supply	2.5 V to 3.3 V

ASG217 overview



The ASG217 circuit is made of 16 identical channels.
Each channel is composed of
- a trans-impedance pre-amplifier;
- a voltage threshold discriminator;
- a 4 bit DAC for threshold adjustment;
- a PseudoLVDS output driver.

In addition a 17th preamplifier with open input may be used as a DC reference voltage.
Three analog signals are available for debugging purpose. These are:
- the channel 0 preamplifier output at one dedicated pad;
- the channel 0 DAC output and the dummy amplifier output multiplexed at a second pad.
Otherwise only the discriminator logical outputs are available at chip pads.

A control logic state machine completes the ASG217 chip.

Pin description

IP0-IP15	IN, analog	Pre-amplifier inputs
VNx-VPx [x = 0..15]	OUT, PseudoLVDS	Discriminator outputs
VDISC	IN, analog	Discriminator threshold
IREF	IN, analog	Preamplifier bias setting, (external resistor to ground)
AOUT	OUT, analog	Auxiliary analog output
AOUT0	OUT, analog	Preamplifier output of the channel 0
TEST	IN, analog + pulldown	Test input also used as a logic reset (see the control section)
CLK	IN, CMOS + pulldown	Clock
CM	IN, CMOS + pulldown	Mode control
DIO	IO, CMOS	Serial data port
VDDA (2 of them)	power	Analog pre-amplifier section
VCC1	power	Analog discriminator input section
VCC2	power	Analog discriminator output section
VDD (3 of them)	power	Digital power (PseudoLVDS drivers and CMOS logic sections)
VSSA (3 of them)	ground	VDDA ground
VSSC (3 of them)	ground	VCC1 and VCC2 grounds
VSS (3 of them)	ground	VDD ground
VSSF (2 of them)	ground	Frame ground

Analog settings

Power down mode

The ASG217 circuit may be switched off to power saving mode. This is the case after a power on reset is done (see the control section thereafter). When in power saving mode the discriminator section is shutdown and the PseudoLVDS driving current is limited around 0.2 mA. The amplifiers are still operational, thus maintaining the input polarizations, if required.

IREF: preamplifier mirror current reference

The preamplifier internal current reference is set through an off chip resistor. The recommended value for this reference is 50 uA. This yields a voltage at the IREF pad close to VDDA - 1.2 Volts. The grounded resistor value is therefore computed from the formula:

$R(IREF) = (VDDA - 1.2) / 50\ 10^{-6}$ KOhms

This results in external resistor values of 44 KOhms at 3.3 Volts and 60 KOhms at 4.0 Volts.

IREF should be in the range 40 - 75 uA. Increasing IREF mainly decreases the noise due to the input capacitor. Decreasing IREF reduces the analog power consumption (at the expense of the increased noise) in the same ratio.

Noise and input impedance versus IREF

Noise decreases when the IREF current increases. Roughly (high gain, high BW):

dVrms = V[iref@50uA] * (50 - IREF) / 100

Input resistance increases when the IREF current increases. Roughly:

dRin = Rin[iref@50uA] * (IREF -50) / 30

Noise and input impedance versus VDDA

Noise increases when the VDDA supply voltage increases. Roughly (high gain, high BW):

dVrms = V[vdda@3.3V] * (VDDA - 3.3) / 9

Input resistance decreases when the VDDA supply voltage increases. Roughly:

dRin = Rin[vdda@3.3V] * (3.3 - VDDA) / 2

Preamplifier inhibit

Each preamplifier can be individually inhibited. Its gain drops down, and the output voltage too.

Discriminator threshold and hysteresis

The voltage threshold at each discriminator is derived from the shared VDISC voltage input combined with individual DAC output. The DAC is 4 bit in range. The DAC voltage range (say VDAC) is programmable to be either 280 mV or 150 mV. These are typical values with a ±10% accuracy. Given N (N within the range 0 to 15) the DAC programmatic value, the discriminator threshold is computed by:

VTH = VDISC - (N/15) * VDAC

The DAC is actually built of 4 current switches of weight 8, 4, 2 and 1. One DAC current consumption reaches its maximum for the programmatic value 15. It is noteworthy that the VDISC voltage input may eat up significant current (up to 2 mA) depending on DAC settings. The VDISC net layout exhibits a 20 Ohms resistance from channel 0 to channel 15. Together with the accumulated current consumption along this path, this induces a slight voltage drop from the computed one. For example assuming a 1 mA total current sink, the maximum (channel 0 to 15) drop would be 20 mV. In most cases this can be neglected. If necessary this can be compensated for by the software, since it is fully deterministic.

The discriminator hysteresis is programmable to be either 12 or 30 mV. These are typical values with a ±15% accuracy.

TEST input

The TEST pad is actually a dual funtion pin: logic reset (when high) and current injection test. For analog test purposes the TEST input drives an injection capacitor at each preamplifier input. Typically a 500 mV (@ 10ns) edge at the TEST input yields a 150 mV peak analog output. The test injection capacitors must be enabled in the global control register (see next). When used for analog test the voltage must be less than 1.0 V. The minimum RESET (active high) level is 2.0 V.

Control logic

Logic block overview

Internal registers are:
- 2 global control registers,
- channel control register per channel, 16 of them.

Global control register1 format (address 16, see next)

bit	
0	Odd test enable (active H)
1	Even test enable (active H)
2	Gain selection (half gain active H)
3	Auxiliary analogue output selection 0 = 17th dummy amplifier 1 = channel 0 DAC output
4	Power up (active H)

Global control register2 format (address 17, see next)

bit	
0	DAC range (0=150mV, 1=280mV)
1	Discriminator hysteresis (0=12mV, 1=30mV)
2	Bandwidth selection (half bandwidth active H)

Channel control register format (addresses 0 to 15, see next)

bit	
0-3	DAC value
4	Preamplifier inhibit input (active H)

During detector readout the logic must be kept quiet (in particular the clock must stop) to prevent noise from being generated.

Logic initialization

At power up, the TEST input must be activated (High) for resetting the internal logic. In normal operation the TEST input must be low. Following the initialization, all registers are reset to zero. *After resetting the logic, the ASG217 is therefore in power saving mode and not operational. First of all the global control register 1 must be written into to switch the ASG217 into power up mode.*

Writing in

Each register is assigned an address and can be individually written into. Address map is:
- 0 to 15 for the dedicated channel control registers;
- 16 and 17 for the global control registers 1 and 2.

Data bits are serially shifted in according to the following sequence.
- CLK starts, MODE is Low.
- MODE input is pulsed High for *one* clock. This signals the ASG217 that shifting in has been initiated.
- 11 bits must follow in that order:
  - at least one start bit (High),
  - 5 data bits,
  - 5 address bits.

Reading out

The global control registers cannot be read out.
The channel control registers can be read out concatenated all together in a single circular 80 bit register.

Data bits are serially shifted out according to the following sequence.
- CLK starts, MODE is Low.
- MODE input is activate High (for *more than one* clock period). This signals the ASG217 that shifting out has been initiated.
- 80 data bits are shifted out, channel 15 inhibit first, then down to channel 0 DAC LSbit.
- MODE gets back Low to stop shifting.

It is noteworthy that during the shift the channel control registers are actually internally shifted, too. After 80 clocks all bits have been rotated and are back to their pre-reading state. Should the sequence be incorrectly implemented then all bits are mixed up (not completely or over rotated).

Electrical characteristics

VDDA pre-amplifier power voltage	3.3 V - 4.0 V
VCC discriminator power voltage	2.5 V - 3.3 V
VDD logic power voltage	2.5 V - 3.3 V (VDD = VCC is recommended)
VDDA supply current	typ. 17 mA @IREF=50 uA
VCC supply current	typ. 8 mA, 0 mA @PWDown
VDD supply current	typ. 44 mA @VDD=2.5 V; 48 mA @VDD=3.3 V; 4 mA @PWDown
VDISC current consumption	2 mA max.
IREF input current	40 uA min., 75 uA max.
TEST input voltage for logic resetting	2.0 V min.
CLK, DM input	CMOS
DIO output	CMOS, @2 mA max. driving current
PseudoLVDS receiver load	100 Ohms typ. off chip
PseudoLVDS driving currrent	2 mA min.
PseudoLVDS common mode, typ.	1.0 V @VDD= 2.5V, 1.2 V @VDD= 3.3 V
PseudoLVDS output resistance, typ.	50 Ohms @VDD= 2.5V, 30 Ohms @VDD= 3.3 V
Analogue outputs current (AOUT, AOUT0)	100 uA max.
Analogue output resistance (AOUT, AOUT0)	50 Ohms typ.
Injection Capacitor	50 fF typ.
TEST input serie resistor	500 Ohms typ.
TEST pulldown resistor	24 KOhms typ.
Preamplifier offset (analog base line)	1.5 V typ.
Preamplifier offset power supply	max. 1% from 3.3 to 5.0 V

sensitivity	
Preamplifier offset temperature sensitivity	max. 5 mV/degree
Preamplifier offset when inhibited	1.0 V max.
DAC output power supply sensitivity	5% from 2.5 V to 3.3 V

Switching time information

Input event rate	20 MHz max. per channel
CLK frequency	50 MHz max.
PseudoLVDS output rise/fall time	4 ns max. @Cld=20pF
DIO output rise/fall time	3 ns max. @Cld=20pF

Die layout